

Design and Implementation of a High Resolution CMOS X-Ray Imager with Amorphous Selenium Sensor

by

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A thesis
presented to the University of Waterloo
in fulfillment of the
thesis requirement for the degree of
Master of Applied Science
in
Electrical and Computer Engineering

Waterloo, Ontario, Canada, 2015

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Abstract

This thesis presents a novel system for high resolution X-ray imaging in medical and industrial applications. Complementary metal-oxide-semiconductor (CMOS) technology is a standard technology used in most state of the art electronic systems including imagers. In addition, amorphous selenium (a-Se) is a photoconductor that is sensitive to a wide range of X-ray photon energies.

Increasing the effective spatial resolution is one the primary goals of state of the art imaging systems. The objective of this thesis is to integrate the a-Se sensor and CMOS readout to make an ultra high resolution X-ray imager. Other features of the imager like noise, dynamic range, imaging speed, and fill factor are competitive with existing X-ray imaging systems. All of the signal reading circuitry is implemented on a custom CMOS chip and the a-Se sensor is deposited on top of it through post processing. This thesis also describe the design of external hardware and software needed to properly operate the imager.

We demonstrate our imager with a 64×64 pixel array prototype containing $5.6 \times 6.25 \mu\text{m}^2$ and $11.2 \times 6.25 \mu\text{m}^2$ pixel. Our results include characterization of the electronic and X-ray imaging performance of our system. We also show X-ray images with effective resolution down to $14 \mu\text{m}$.

Acknowledgements

First and the most important, I would like to thank my family; Shima, mom and dad many times for the support they provided me through my entire life. It is hard to describe with words but all I can say is this project as well as any accomplishment in my life was not possible without their support.

Thanks to my both supervisors Prof. Peter Levine and Prof. Karim Karim for their support. They put enormous amount of time and energy for theoretical and practical complications during this project. Also I like to thank Prof. Chris Backhouse and Prof. David Nairn for reviewing this thesis.

I would like to thank our research team students specially Abdallah El Falou and Chris Scott. They worked on this project directly and their incredible knowledge helped me a lot.

Also I have to mention Rasoul Keshavarzi for his help during these two years. I have to thank Prof. Michael Mayer and his student Jimy Gomes who provide their wire bonding technology and solutions.

Also I would like to thank Richard Barber for providing a cleanness and safety in the G2N lab. Additional thanks to Electrical and Computer Engineering staff at University of Waterloo who have huge direct and indirect impact on students mental and physical conditions and provide an environment for research and study.

Dedication

This is dedicated to my family.

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Chapter 1

Introduction

X-rays were discovered by Wilhelm Rontgen in 1895. X-ray photons pass through some materials that visible light cannot pass, and this feature opens up a way to see objects that visible light cannot show. X-rays cannot penetrate dense materials and penetration percentage depends on X-ray photon energy as well. This feature brings up the opportunity to get images that only show denser objects.

Important applications of X-ray imaging in science and industry include non-destructive testing (NDT) and biomedical imaging. NDT involves observing an object without damaging its functionality and is used extensively in aircraft manufacturing and the oil and gas industries. X-ray imaging is also used in lots of biomedical applications. Several examples are mammography, which is breast cancer diagnosis; computed tomography, which is generating cross sectional images of body organs; and fluoroscopy which is, real time imaging for diagnostic processes. Because X-ray photons have higher energies than visible photons, they can harm living cells when they interact with organic structures. This interaction brings up the concern about X-ray imaging damage to the human body. As a result, X-ray exposures with lower dosage are preferred to reduce the potential harm.

Decreasing X-ray flux means decreasing the signal level in the image and this results in a lower signal-to-noise ratio (SNR). At a certain X-ray input dose, the level of signal that includes information would be equivalent to the level of system noise. Below this level, the information is buried in the noise. Therefore the noise level determines how low an X-ray dose can be provided.

Another important characteristic of X-ray imagers in medical and NDT applications is spatial resolution. Spatial resolution defines the minimum detectable object size of the imager.

This thesis presents the design and implementation of a high spatial resolution X-ray imager, obtained by the combination of complementary metal-oxide-semiconductor (CMOS) technology and amorphous selenium photoconductor. This thesis also describes the potential and limitations of this technology for the next phases of this research.

1.1 Introduction to X-ray Physics

Photons are described by their energy or wavelength. Figure 1.1 shows where X-ray photons are located in the electromagnetic spectrum. The range include wavelengths between $0.1 \mu\text{m}$ to 0.01 nm . In X-ray applications, it is usual to report the energy by kilo electron volt (keV) unit which is $1.6 \times 10^{-19} \text{ J}$. Also, X-rays are divided in two ranges. X-ray photons with energy less than 3 keV are called “soft” because they easily get absorbed by water and air. X-rays with energies more than 3 keV are called “hard” and penetrate materials depending on their energy[17].

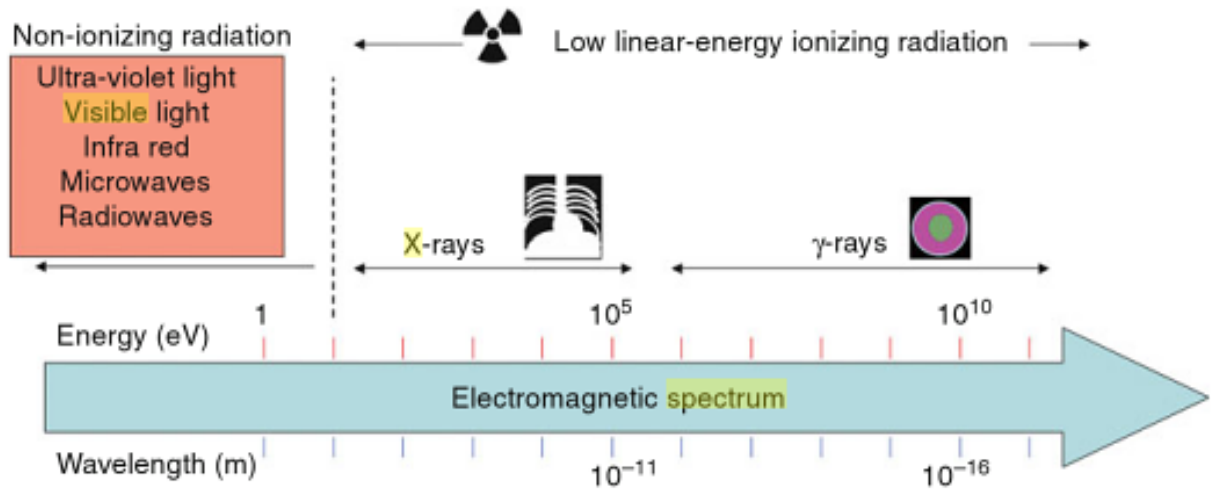


Figure 1.1: The electromagnetic spectrum (from [16]).

Figure 1.2 shows one procedure to generate X-rays. A voltage source produces a potential energy between a cathode and anode in a tube. By increasing this potential, the electric field in the anode increases to the point that the force from this field overcomes the material potential such that electrons from the cathode (which is commonly made from tungsten) get projected and accelerated toward the anode. Typical anode materials are W, Mo and Rh. As the electrons collide with the target (anode), X-ray photons are produced and projected from the collision point. The emitted X-rays usually pass through a filter before interacting with an object to be imaged. The collimator makes the directions of X-ray beam more aligned in a specific direction for imaging. A detector is placed below the object to absorb X-rays in different spatial locations to produce an image.

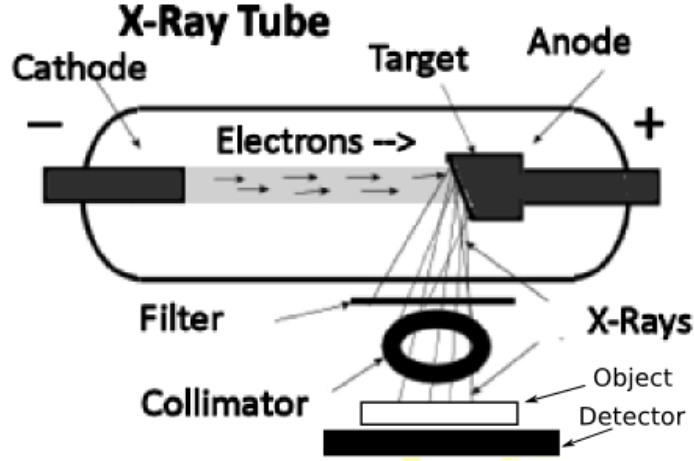


Figure 1.2: Production of X-rays in a tube (adapted from [15]).

Photons generated in this way have range of energies. The maximum energy E_{max} is given by $E_{max} = qV_{tube}$, where V_{tube} is the tube potential (usually given in units of kiloVolts peak (kV_p)) and q is the electronic charge. The other characteristic of X-ray photons is their distribution on the energy band which depends on the target material and tube voltage[7]. There are several standard targets and each produces a specific histogram of photon energies. This histogram shows the relative number of generated photons in each energy bin. As shown in Figure 1.3, the filter shapes the distribution as well to reduce low energy photons.

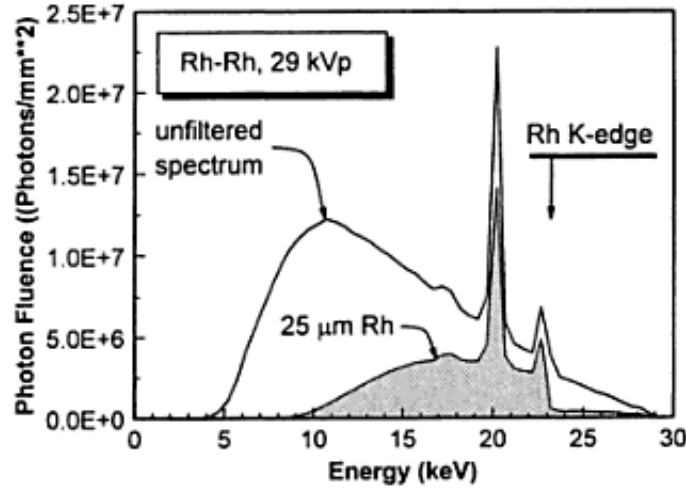


Figure 1.3: A rhodium anode spectrum with 29 kVp source before and after filter is shown (from [5]).

The conventional unit used for radiation exposure is the Roentgen (R). When X-ray photons travel in air they can interact and ionize the air. 1 R is the amount of exposure that produces 2.58×10^{-4} C of ionization per kilogram of air under standard temperature and pressure. An exposure value can be converted to photon fluence which is the total number of photons per unit area. But the conversion factor depends on X-ray energy because the probability of interaction with air and number of ionized particles is different for each energy. For example, for 60 keV X-ray photons, 1 R is equal to $3.1 \times 10^{10} \frac{\text{photons}}{\text{cm}^2}$.

1.2 X-ray Imager Technologies

1.2.1 Analog vs. Digital Imaging

X-ray imaging techniques are divided into two different categories: film/screen and digital imaging. In the early days of X-ray imaging, a film was exposed to the X-rays after passing through the object. After that, the exposed film was processed to reduce the silver ions to metallic silver [49]. In this method, the data acquisition, storage and display are all in same process and completely correlated. Any problem during one of these steps effect other ones. Also wet post processing facilities are necessary to make the image ready to use. On the other hand, digital imaging detectors utilize a sensor converting the X-ray photons to charges due to the generation of electron hole pairs . These charges result in a voltage or current and they can be detected by a pixel readout circuit. This electrical information can be stored in digital format. The display is completely separated and the data can be processed and displayed later from the saved values. When first introduced, digital technology had two serious problems. First one was the noise associated with the electronics that corrupts the signal, and the second one was the resolution of imaging because of large size of digital pixels. These problems were addressed later and as a result, digital imaging became the trend for X-rays and also visible light imaging.

1.2.2 Direct vs. Indirect X-ray Conversion

There are two different methods of X-ray conversion to electron and hole pairs. The first and simpler way is to use a material which transforms the X-rays to charge directly. This method is called “direct conversion” and the most well-known material used in this method is amorphous selenium (a-Se). Amorphous selenium is manufactured using low-capital-cost equipment, can be processed over a large area, and has the lowest dark current of commonly used photosensing materials at room temperature (e.g., Si, a-Si, Ge, and HgI₂) owing to its amorphous nature and 2.2 eV bandgap. Moreover, it exhibits an inherently high spatial resolution (on the order of 5 μm) for X-ray photon energies between 20 and 40 keV [14]. On the other hand, in indirect conversion, an intermediate step is introduced in which the X-ray photons are converted to visible light in a scintillating medium and then the light is converted to charge using a sensor. For this method, usually caesium iodide (CsI) is used as scintillating material and, in some cases, gadolinium oxysulfide (Gd₂O₂S) is used [10]. The drawback of indirect conversion is that light spreads in every direction in the scintillator and results in loss of spatial resolution. Reducing the sensor thickness

decreases this effect, but low thickness results in low X-ray absorption. So the direct X-ray conversion potentially results in higher modulation transfer function which means better spatial resolution. Also, a huge advantage of direct conversion is simplicity and low cost of the design compared to the indirect method.

1.2.3 Readout Technologies

The X-ray sensor only converts X-ray photons to an electronic signal. The next important component is the readout system. Although the readout system includes many components, the first and most critical one is the pixel. There are three main technologies for pixel implementation; thin film transistor (TFT), charge coupled device (CCD) and CMOS. Comparing to CMOS and CCD devices, TFTs can be developed in a much larger area in standard manufacturing companies. The other benefit is also the very low cost per unit area. The main disadvantage of TFT circuits comes from the relative inaccurate process compared to CMOS. In addition, TFT device mobilities are much lower than CMOS transistors and TFT transistors are much larger than CMOS transistors, so the minimum pixel area is higher compared to the other technologies.

Before 1990, CCDs had a huge advantage in respect to CMOS including uniform response and superb image quality. After major improvements in lithography, however, CMOS circuit designers took advantage of this and started to develop CMOS imagers to compete with CCDs. Now, both are in mainstream. The reading mechanism in CCD is to transfer the charge stored in each pixel to the adjacent one by changing the voltage levels at metal electrodes and serially reading the output. CCDs are usually custom processes where integration of additional analog/mixed-signal circuits is difficult. We choose CMOS for its small feature size and flexibility in design. CCD imagers consume more power than CMOS because of frequent gate switching. Because the pixel plays an important role in the system performance, we now explain the most well known CMOS pixel designs.

1.3 Pixel Architectures

In CMOS technology, there are a variety of pixel architectures. Depending on the application, the designer can choose the most suitable one. These architectures are mostly used for imaging based on a photodiode in a pixel and are described next.

1.3.1 Passive Pixel Sensor (PPS)

The passive pixel sensor (PPS) contains one transistor per pixel (1T) as shown in Figure 1.4. The operation is fairly simple because the transistor acts like a switch. When the gate of the transistor has low voltage, it is off and the sensor charges the capacitor at the integration node when photons strike the photodiode. After the integration phase, the transistor gate voltage flips to high and the switch is on. Then the accumulated charge at this capacitor is forced to discharge because of the virtual ground provided by the op amp at the end of the column. This charge is then integrated on a capacitor C_F and the voltage at column amplifier output is ready to be read.

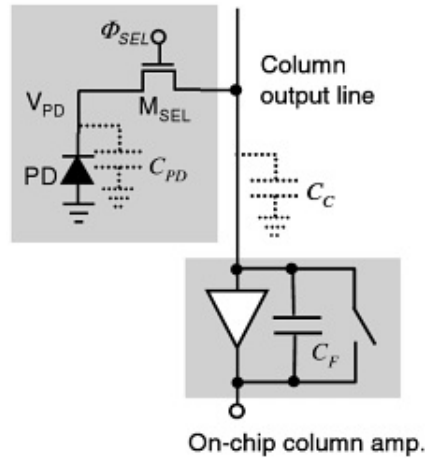


Figure 1.4: PPS Pixel and integrator. Taken from [30].

The main advantage of this pixel architecture is small area. For the structures which implement the sensor in CMOS layers it features high fill factor which is defined as the ratio of photon sensitive area to the total area of the pixel. However PPS image quality is really low because of low signal to noise ratio (SNR). The reason is the huge column capacitor and the interference of this capacitor in charge transfer mechanism. The sampled

noise as charge on column capacitor is $Q_n^2 = kTC_C$. So the SNR can be calculated as

$$SNR = \frac{Q_{signal}^2}{kTC_C}. \quad (1.1)$$

So bigger column capacitor results in lower SNR.

1.3.2 3T Active Pixel Sensor (APS)

This structure is a solution to the noise problem in PPS. In this structure, three transistors are used in each pixel. Figure 1.5 shows this structure. The operation in this pixel is more complicated compared to a 1T pixel. At the beginning of each cycle, the M_1 transistor which acts as a switch turns on and the capacitance voltage at sensor node resets to V_{dd} . After reset, this switch turns off and the integration starts. The phase after integration is reading phase which starts with turning the M_3 on to address the row. Select transistor acts like a switch and when it is on M_2 transistor is biased by a current source at the end of the column and operates in the saturation region as a source follower.

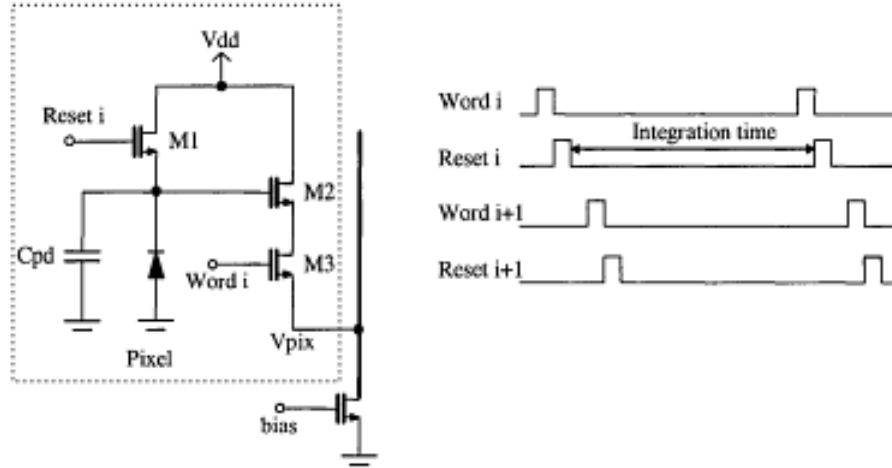


Figure 1.5: 3T pixel with photodiode sensor and timing diagram [31].

The good feature in 3T structure is a better noise performance and high speed read operation which can be important in some applications. Here the noise voltage is usually limited to kT/C_{int} in which C_{int} is the total capacitance at integration node. Also, the fill factor is less than PPS in the structures which use CMOS photodiode or photogate.

1.3.3 4T Active Pixel Sensor

A 4T APS is shown in Figure 1.6. This pixel is similar to the 3T structure but the fourth transistor, TG, is added between the gate of source follower transistor and sensor integration node. The sensor is a pinned photodiode which uses p+, n, and p layers. The p+ and p regions both are connected to ground. Doping of these regions and width of the n region is designed so that when the voltage is applied to the n region, the depletion regions from both pn junctions grow toward each other and, at a certain voltage V_p , these depleted regions meet and the device is fully depleted. At this point the potential cannot increase any more.

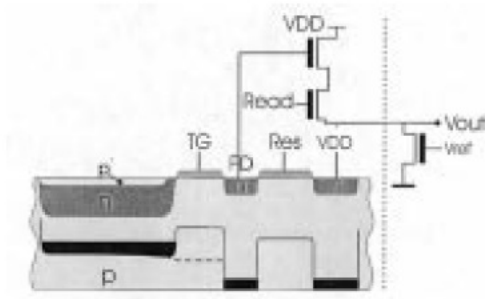


Figure 1.6: Pinned photodiode structure in a 4T pixel (from [26]).

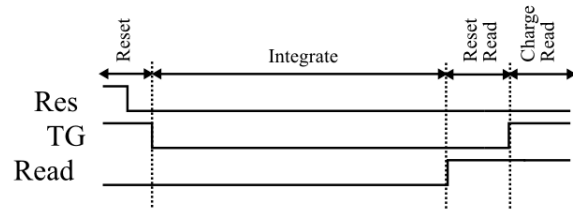


Figure 1.7: 4T APS pixel timing diagram.

Before integration, both TG and Res transistors are on and the pinned photodiode is depleted. After that, the Res and TG turn off and integration starts. Electron and hole pairs generated from incoming photons decrease the voltage at n region. At the end of charge integration, before turning on TG transistor, the first read happens to read any noise and offset voltage from the gate of source follower. Then TG opens and full charge transfer happens between two nodes and the n region goes back to full depletion. This full charge transfer concept is very important and this feature comes from the fact that this junction voltage is pinned and cannot increase more than V_p . At this moment the second read happens and the subtraction between these two reads is the final result. One advantage of this pixel architecture is that it provides read noise reduction through correlated double sampling (CDS) [29].

1.4 X-ray Detector Performance Metrics

To measure an imager system performance some standard metrics and features need to be explained briefly. Nominal resolution is determined by the size of the pixels. The effective resolution is the final object determination power of the system which takes nominal resolution and some other factors into account. The effective resolution is always worse or equal to the nominal resolution. The density of pixels can be increased by scaling down the pixel area. However, this scaling impacts the rate at which the whole array can be read (known as the “frame rate”), assuming a constant pixel integration time. The significance of an imager frame rate becomes crucial in video applications like tomosynthesis mammography.

1.4.1 SNR, LOD and DR

The first important property is (SNR) which shows the ratio of useful information to noise and plays an important role in image quality. The minimum signal that can be detected by the imager is called limit of detection (LOD) and noise plays an important role in this metric. LOD is often defined as input power that results in $SNR = 1$. Dynamic Range (DR) for an imager is defined as the difference between two limits. The bottom limit is the LOD and the top limit is the input power that saturates the imager.

1.4.2 MTF and DQE

Modulation transfer function (MTF) is similar to the LTI system frequency magnitude response $|H(j\omega)|$ but instead of time domain, spatial domain response is the focus. Figure 1.8 shows the concept behind MTF. If the object to be imaged consists of line pairs defined as ideal black and white bars in spatial domain then the input of the system is a square wave with full contrast between two phases. The ideal system has same contrast at its output, which is the image. But real imaging systems exhibit reduced contrast depending on the effective resolution. As lines get closer to each other (higher frequencies in spatial domain), the imaged contrast gets lower. Figure 1.9 shows an example of a typical MTF curve. The MTF curve of a higher resolution system drops at higher frequencies.

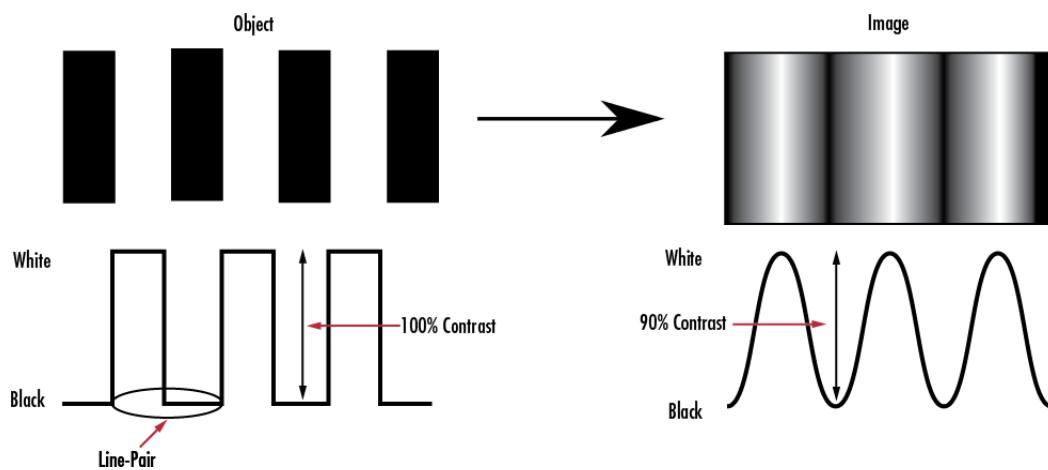


Figure 1.8: Concept of MTF (adapted from [1]).

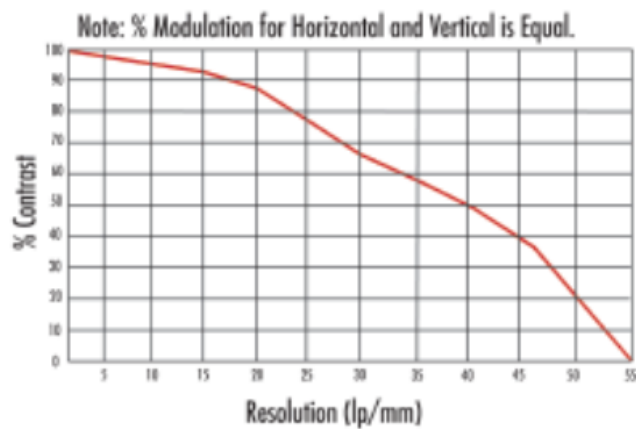


Figure 1.9: An example of MTF curve

The other metric in imager systems is detective quantum efficiency (DQE). The interpretation of DQE is a parameter that shows the efficiency of transferring information from input of the system to output of the system as a function of spatial frequency.

1.5 Motivation and Objectives

Resolution of an imager determines the smallest detectable object. The object size limitation is really crucial in some applications. The importance of high resolution in biomedical applications like chest X-rays relies on determining cancerous tumors at early stages [32]. This demand led researchers to build higher resolution X-ray imaging systems to reduce pixel pitches to less than 200 μm . However the effective resolution enhancement is not accomplished only by pixel pitch reduction because of other limitations. For example, each X-ray produces a cloud of charge after absorption by the sensor [3] and if the charge cloud is greater than pixel size then decreasing pixel size does not help the resolution. This is where a combination of CMOS and a-Se as direct converting material becomes important. As explained, in direct conversion imaging the problem of light spreading in scintillator does not exist and also in CMOS technology less than a micrometer pitch for pixels is possible to design. Also it, is shown in previous work like [51][18], the combination of direct X-ray conversion materials and high resolution CMOS or CCD readouts can lead to high spatial resolution readout.

Amorphous selenium is characterized well in STAR group at University of Waterloo, but now we want to utilize this technology and design our own imager with freedom of optimization. Also we want to push forward the resolution and design an imager with smaller pixels. Our goal is a pixel pitch around 5 μm with an imaging system operating up to 60 FPS for video applications. Also, we would like to study the properties of a-Se in a complete imaging system, and not only as a single pixel so that future works can extend this research for special applications such as phase contrast imaging.

Noise performance is crucial in some applications. In CMOS imagers, CDS is often used to reduce one of the important noise source contributors. But CDS was always applied to pixel architectures utilizing pinned photodiode. As discussed in [39], it is possible to use a 4T structure with a conventional (not pinned) photodiode. We have designed both 4T and 3T pixels and we like to study the noise performance in each one.

Our objective is to build a monolithic X-ray imager that combines an a-Se sensor and CMOS pixel array with high spatial resolution. We will evaluate the effective resolution of this imager and will investigate the SNR performance of several pixel variants.

1.6 Organization

In Chapter 2, the design of the imager is discussed. First the amorphous Selenium features are explained. After, the chip design is explained in details which includes pixel structures, digital control circuitry and on-chip buffer. Important specifications are calculated based on the theory and compared with required performance. At the end the design of extra necessary hardware and software is presented with details.

In Chapter 3, the experimental setup of this system is explained. Then, important measurements are discussed and important features of the system are shown based on these measurements. We have discussed temporal noise, fixed pattern noise, modulation transfer function as well as linearity of the response are expressed based on the measurements. Moreover, X-ray images taken from this system are shown at the end of this chapter.

In Chapter 4 a conclusion is made based on the system performance. Unachieved performances based on measurements and possible solution are discussed in this chapter. At the end, the future work of this research and the potentials to extend this project are mentioned.

Chapter 2

Design

The design flow of the proposed a-Se/CMOS imager and supporting hardware is now presented. Figure 2.1 shows the block diagram of the complete imaging system and Figure 2.2 shows the signal flow. We can separate these blocks into three major components. The first component includes the sensor, pixel array, controllers and buffer which are located on a custom CMOS chip. The second component includes buffer, filter, analog-to-digital converter (ADC) and a field programmable gate array (FPGA) implemented on a custom printed circuit board (PCB). The third component is system software.

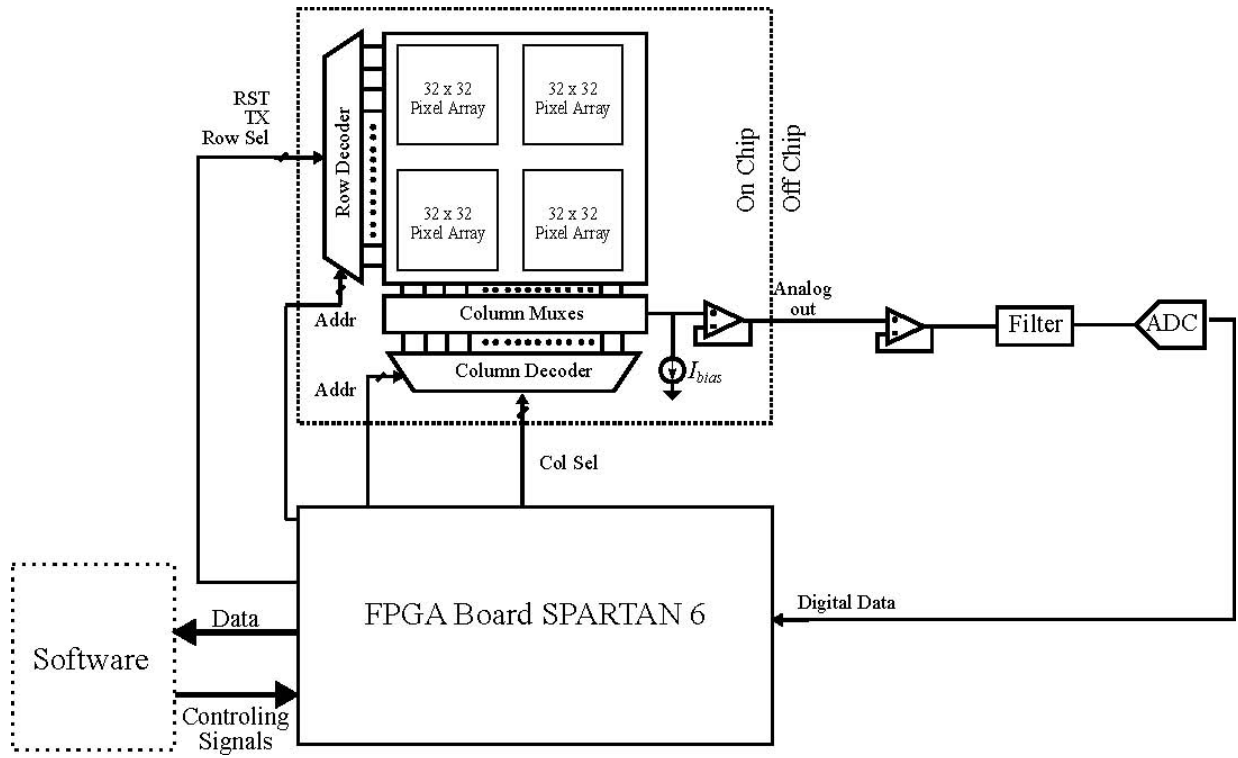


Figure 2.1: Block diagram of the X-ray imaging system.

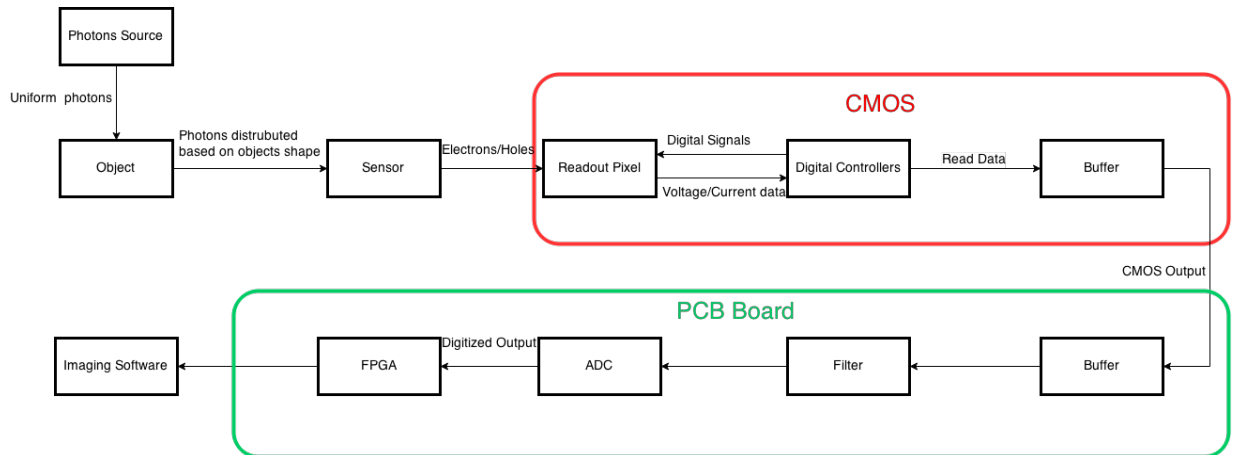


Figure 2.2: X-ray imaging system signal flow.

2.1 Amorphous Selenium Photoconductor

The key specifications that comes with a-Se as detector is that this material can be deposited in large area, having enough thickness with simple deposition methods. So it is really low cost and compatible with CMOS. We can use post-processing techniques to deposit a-Se on the surface of a CMOS chip. For this, we do not need any technology modification which is not the case for imagers that use pinned photodiodes.

2.1.1 Resolution

One of the most important features of a-Se is the good spatial response of this material using direct conversion. As we mentioned, one of major goals of this imager is high spatial resolution. To explain this feature, we can compare it with indirect imagers that use scintillators. When a X-ray photon hits a scintillator, it generates photons and they are absorbed by another detector like Cs-I layer. While these visible photons travel from the scintillator to the detector, they can spread and effect neighboring pixels as well. Decreasing the thickness of detector reduces this effect, but it results in lower X-ray photon absorption. As a result, using a-Se lets us benefit from high spatial resolution and high quantum efficiency.

Another advantage to using a-Se as a photodetector is the high fill factor that can be achieved. This comes from the physical structure of our imager. Pixel fill factor is defined as the area percentage of sensitive portion of the pixel to total area of the pixel. Because a-Se is a uniform layer over all the pixels the fill factor is almost 100%. This feature is very important when the imaging object is human body because in ideal case the imager should use all photons to produce an image. As a result, the same quality of imaging is obtained with smaller X-ray dose. There are solutions to increase the fill factor in indirect imaging systems like introducing micro lenses but the result is a complex manufacturing process and high cost.

Figure 2.3 shows the potential of using a-Se in a detector to get an inherent resolution. It can be seen for an accurate optical setup (solid lines) that an MTF equal to 0.5 occurs at 40 lp/mm. This means 50% contrast for 12 μm thick line pairs. In this figure, we can also see the MTF for two different a-Se thicknesses calculated in theory [36].

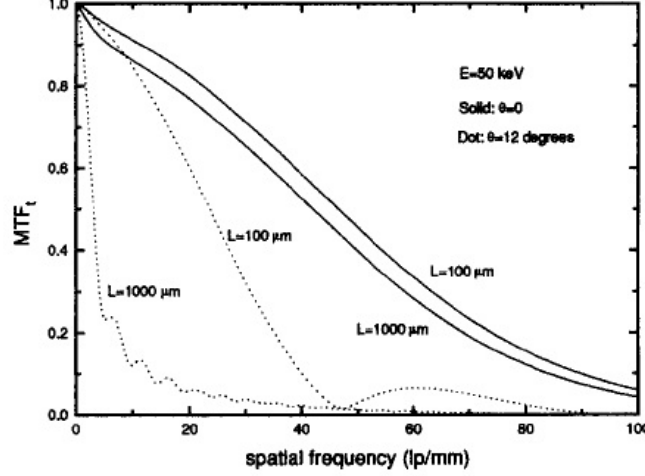


Figure 2.3: A-Se MTF for 50 keV photons for 100 μm and 1000 μm thick layers. θ is the angle between X-ray beam and perpendicular plane an a-Se surface [34].

2.1.2 Dark Current

Another important factor in detectors is dark current. a-Se has very low dark current (10 pA/mm² at 9 V/ μm bias [2]) which is the current that passes through the sensor when no photon hits the detector. This current can increase the pixel output voltage and decrease the dynamic range. Shot noise produced by this current can also be problematic. Using blocking layers reduce dark current [2], but these are beyond the scope of this thesis.

2.1.3 Sensor Gain

The total imager gain G_{total} can be divided into two main components $G_{total} = G_{Sensor} \times G_{Circuit}$, in which G_{Sensor} is the gain between number of incident X-ray photons and electron hole pairs and $G_{Circuit}$ is the gain between electron hole pairs and output voltage read. The gain of the sensor depends on several variables like the thickness of the sensor, biasing voltage, fill factor, and the photon energy. We can define the a-Se gain in two stages: one is quantum efficiency (QE) and the second is conversion gain [20]. QE means the percentage of X-ray photons that interact with a-Se material and can be calculated with Beer-Lambert law in the following equation:

$$\eta_{(E)} = 1 - e^{-\alpha(E)t}. \quad (2.1)$$

Where E is energy of the photon, $\alpha_{(E)}$ is energy dependent linear attenuation coefficient, (product of mass attenuation coefficient and density) and t is material thickness. Figure 2.4 shows mass attenuation coefficient for different photon energies for a-Se and CsI.

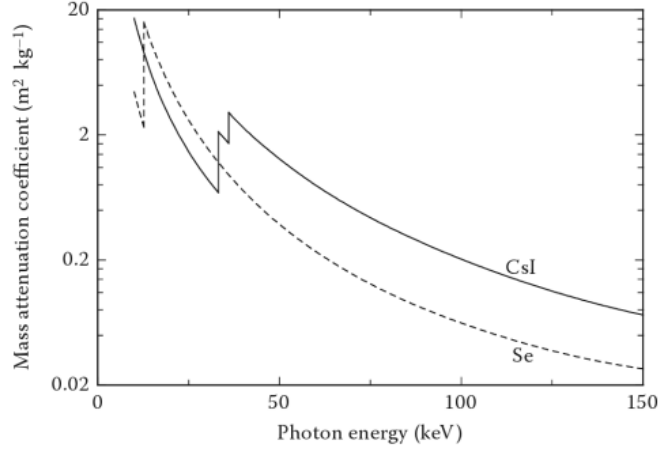


Figure 2.4: Attenuation coefficient of a-Se and CsI versus photon energy [21].

For example for 10 keV X-ray photons $\eta_{(E)} = 0.7$ which means 70% absorption of the incoming photons. Any absorbed X-ray photon releases electrons because of the photoelectric effect. The factor that converts number of electrons hole pairs to number of absorbed photons is the conversion factor $g_{(E)}$ and can be estimated by [22]

$$g_{(E)} = \frac{E}{W_{\pm}}, \quad (2.2)$$

Where W_{\pm} is electron hole pair creation energy obtained from

$$W_{\pm} = W_{\pm}^0 + \frac{B}{F}, \quad (2.3)$$

In which $W_{\pm}^0 = 6$ eV, $B = 4.4 \times 10^2$ eV · V · μm^{-1} and F is the electric field in the a-Se. Now we can see the effect of electric field across the sensor on system performance. For example for 10 keV photons and 5 $\frac{\text{V}}{\mu\text{m}}$ a-Se biasing, $g_{(E)}$ is 106 $\frac{\text{eh}}{\text{photon}}$. If we increase the electric field the loss of the signal would be smaller because gain is higher. The reason is higher electric field results in faster generated electron and hole pairs sweeping in a-Se body. Faster sweeping decreases the recombination of electron hole pairs and signal is

higher in this case. it should be noted that (2.3) is not correct for very high electric fields ($E > 10^8$ V/m) where avalanche multiplication happens [40]. Considering the system level imaging system, the first block is the sensor. And the gain in first block is the most important gain for noise performance in any system. In our system the voltage across sensor is maximum 5 V/ μ m to avoid any risk of breakdown. At this voltage there is no avalanche in the system.

So the sensor gain can be found from the ratio between total number of electrons to number of emitted photons calculated by combining (2.2) and (2.1):

$$G_{sensor} = \frac{N_{e/h}}{N_{photons}} = \eta_{(E)} \times g_{(E)}. \quad (2.4)$$

So in our setup with 60 μ m a-Se thickness and 300 V bias the total gain G_{sensor} is equal to $75 \frac{eh}{\text{photon}}$

2.2 CMOS Pixel Specifications and Design

We have decided to use 3T, 4T and 6T pixels because the reading operation is fast and also the area can be limited for ultra high resolution. We have designed four 32×32 arrays of pixels with different pixel structures in a TSMC 0.18 μ m mixed-signal CMOS process. Two of them are implemented with different 4T pixels, one uses a 3T pixel as a reference and one is a 6T pixel. There are slight differences between these two 4T pixels but they are operated with same timing as explained in introduction. But the main difference here is using a-Se photoconductor instead of photodiode. The 6T pixel operation is like 4T but it utilizes transmission gate instead of single NMOS or PMOS switches. We are developing integration-mode pixels where electron hole pairs (EHPs) generated in a-Se are integrated onto an in-pixel capacitor. On each pixel an opening is designed to make the connection from a-Se to the pixel. This opening is connected to the integration node of the pixel. Note because in a small area pixel the integration capacitor cannot be large, the dynamic range can be limited and it is important to increase it enough for practical use of the pixel. To overcome this limitation, we have used 3.3 V thick gate oxide transistors. Using this type of transistor improves the performance in two different ways. First, because the voltage range is 0 to 3.3 V more photons can be integrated for a given integration time compared to the normal thin oxide devices. The second reason that 3.3 V transistors are better, is related to transistor leakages when they are off. As we mentioned transistor off-state leakage might be a limiting factor in this sensitive design when the capacitor is

very small and also the noise performance is important. 3.3 V transistors feature small leakages compared to 1.8 V devices [46].

2.2.1 Quadrant 1

Quadrant 1 (Q1) contains an array with 4T pixels built using all NMOS transistors. Figure 2.5 shows the schematic and Table 2.1 shows the device information of this pixel. There are two important considerations in this design. The first relates to the source follower transistor. The output voltage V_{out} on a 4T pixel like Figure 2.5 can be calculated as

$$V_{out} = V_{g_{SF}} - V_{g_{s_{SF}}} - V_{ds_{RS}}, \quad (2.5)$$

in which $V_{g_{SF}}$ is the voltage at the gate of source follower which is a function of the input charges, $V_{g_{s_{SF}}}$ is the voltage drop from source to gate and V_{RS} is the voltage drop across row select (RS) transistor when it is on during the reading cycle. Assuming the RS acts as an ideal switch this voltage drop can be ignored and the output voltage can be written as :

$$V_{out} \approx V_{g_{SF}} - V_{g_{s_{SF}}} = V_{g_{SF}} - V_{th_{SF}} - V_{OV_{SF}}, \quad (2.6)$$

Where $V_{th_{SF}}$ is the threshold voltage and $V_{OV_{SF}}$ is the overdrive voltage of source follower transistor. As can be seen in 2.6, the threshold voltage of source follower limits the dynamic range of the pixel. Any voltage less than the threshold voltage at the gate of source follower transistor results in weak inversion region of this transistor. This voltage drop should be minimized to increase the dynamic range. Native transistor is a transistor with an almost zero threshold voltage. If a native transistor is used for the source follower then the dynamic range can increase, especially when the transistor is a thick-oxide device which has a threshold voltage around 1 V. The drawback of using this transistor is more area consumption and also lower transconductance g_m for a given bias current and aspect ratio. The area can be a serious concern in this situation but it is not the case for our system because the dominant limiting factor is the capacitance layout that will be explained later.

Another feature available in this technology is metal-insulator-metal (MIM) capacitors. These are made using a special metal layer between metal 5 and metal 6, located very close to metal 5, designed especially to provide a capacitance density of 1 fF/ μm^2 . So we can achieve higher capacitances for small pixels using MIM capacitors but the problem is the minimum size of these capacitors. Design rule files let us to have a minimum 4 $\mu\text{m} \times 4 \mu\text{m}$ layer of this metal layer. Also we need to get connections from this capacitor to the other nodes of the circuit. Because of fabrication limitations connection from metal 5 on this

capacitor can only be made out of the area of the cap covered by MIM layer, so metal 5 sketch should be wider than 4 μm so that a connection can be made at that location. Also the MIM layer connection is only allowed to metal 6 and this metal need to be connected to other metals down. As a result the metal 6 needs an area without the metal 5 under it so that the connection can be made. Because of these layout limitations based on design rule check (DRC) the smallest pixel area we could get with a MIM capacitor is 5.6 $\mu\text{m} \times 6.25 \mu\text{m}$. This area is more than the minimum pixel size that we can achieve without the MIM capacitor. Because of this the transistor sizes are not chose as minimum as they can, which is 220 nm for width and 180 nm for length.

In Q1 pixels, there is a 17.6 fF MIM capacitor at the integration node to increase the dynamic range, linearity and also for avoiding variations in node capacitance due to parasitics. The source follower is a native transistor to avoid dynamic range reduction. The reverse biased diode is necessary to protect and limit the voltage at integration node. Without this diode, the integration capacitor voltage could rise until the gate of the CMOS devices break down. To avoid any danger, the diode is connected to 3.3 V to limit the voltages more than $3.3 + V_{th_{diode}}$. The controlling systems work exactly like we described for a general 4T pixel structure.

Component	Type	Specification
M_{TX}	NMOS	W/L = 1 $\mu\text{m}/0.50 \mu\text{m}$
M_{RST}	NMOS	W/L = 1 $\mu\text{m}/0.35 \mu\text{m}$
M_{SF}	native NMOS	W/L = 1.20 $\mu\text{m}/1.20 \mu\text{m}$
M_{RS}	NMOS	W/L = 1.20 $\mu\text{m}/0.35 \mu\text{m}$
D_{prot}	PN diode	Area = 0.20 (μm) ²
C_{int}	MIM cap	Capacitance = 17.6 fF

Table 2.1: Quadrant 1 pixel components and sizes

2.2.1.1 Pixel Gain

The sensor provides electrons and holes and after that these charges are integrated on a capacitor C_{int} in Figure 2.5. In Q1, this charge is transferred in reading phase to the gate of source follower. The charge transfer mechanism in this case is a simple charge divider between two capacitors. So the gain at this point is

$$V_{G_{SF}} = \frac{Q_{signal}}{C_{int} + C_{par}}, \quad (2.7)$$

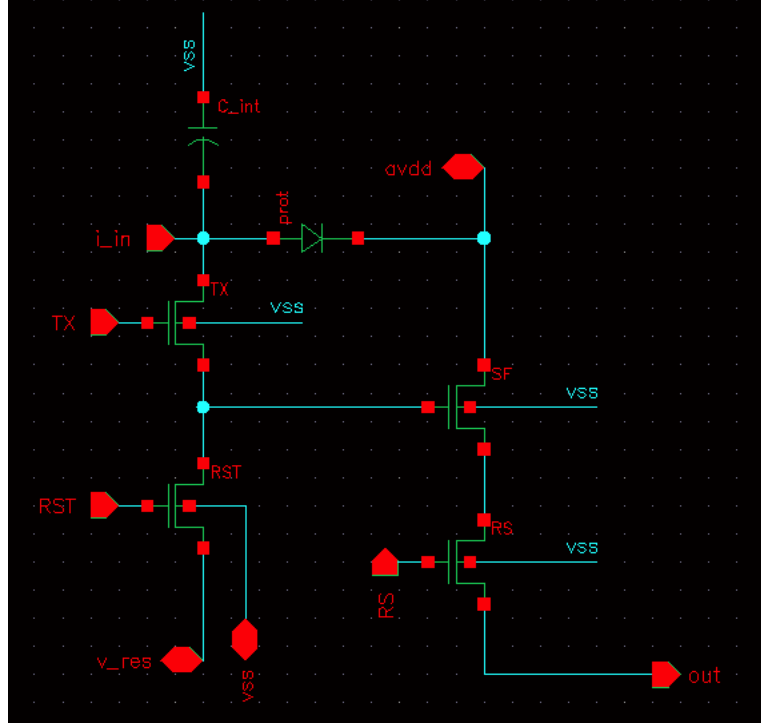


Figure 2.5: Schematic of quadrant 1 pixel.

in which C_{par} is the total parasitic capacitance at source follower gate node and Q_{signal} is the total integrated charge from the sensor. With the small transistor sizes used in these pixels, the parasitic capacitors can be several fF based on Spectre circuit simulations. The next gain step is from gate of source follower to source of this transistor. This gain is given by [37]

$$A_v = \frac{g_m R_s}{1 + (g_m + g_{m_b}) R_s} \approx \frac{g_m}{g_m + g_{m_b} + g_{ds}} = \frac{1}{1 + \eta}, \quad (2.8)$$

in which g_m is transistor transconductance, g_{m_b} models transconductance due to body effect, R_s is to total resistor seen from source of this transistor and $\eta = \frac{g_{m_b}}{g_m}$. In this case, R_s can be estimated with small signal resistance seen from current source transistor drain r_o and it is over 1 M Ω . For typical source-bulk voltages, η remains greater than 0.2[37]. This gives a gain around $0.8 \frac{V}{V}$. But for native transistors, η is around 0.05 based on simulations and the source follower gain is therefore close to $1 \frac{V}{V}$. Combining (2.7) and

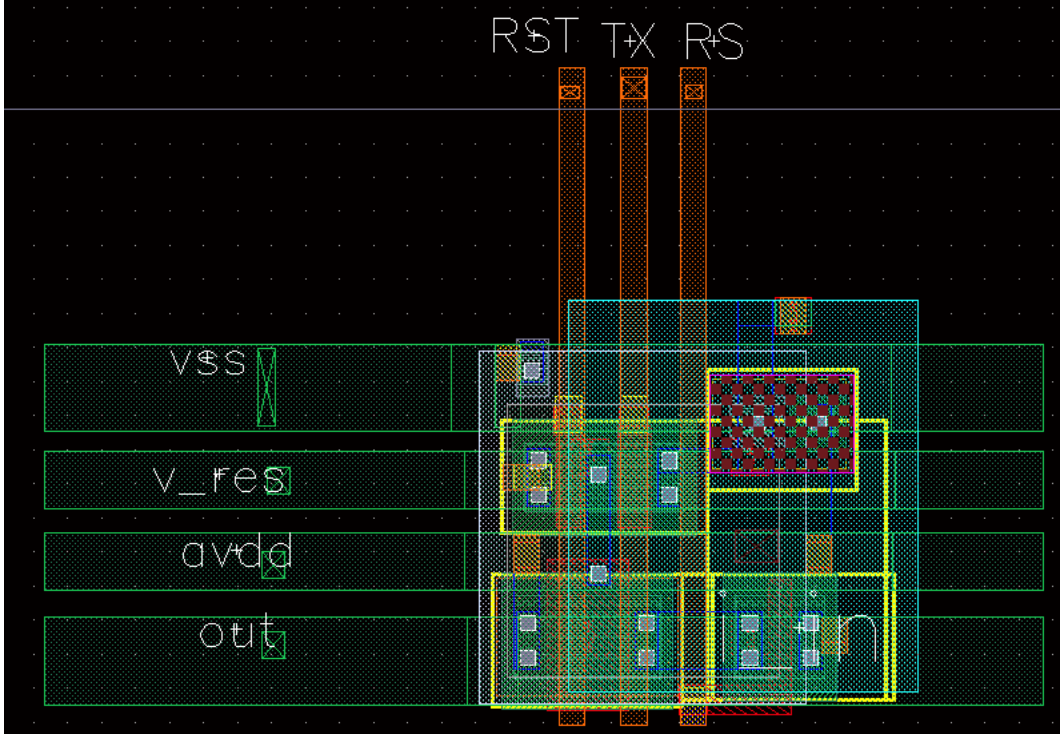


Figure 2.6: Layout of quadrant 1 pixel.

(2.8), The overall pixel gain G_{Q1} is

$$G_{Q1} = \frac{q}{C_{int} + C_{par}} \times \frac{1}{1 + \eta} \approx \frac{1.6 \times 10^{-19} C}{30 fF} = 5.33 \times 10^{-6} \text{ V/e}^-. \quad (2.9)$$

2.2.1.2 Pixel Noise Performance

There are two different categories of noise in pixel architectures: temporal and spatial. Temporal noise is random variation of the pixel value versus time and spatial noise is the variation of the output between different pixels which does not vary with time. Main temporal noise sources in a pixel are thermal, flicker and shot noise. Computing all noise sources and measuring them is beyond the purpose of this research but the main ones are introduced.

The first noise source in a readout pixel is thermal noise. The thermal noise voltage

power spectral density (PSD) of a resistor is

$$V_n^2(f) = 4kTR, \quad (2.10)$$

in which k is Boltzmann constant, T is temperature in Kelvin, and R is the resistor value. For the MOS transistor in triode region, the thermal noise can be modelled as a current source between drain and source with the value of [8]

$$I_n^2(f) = \frac{4kT}{R_{DS}}, \quad (2.11)$$

where R_{DS} is the channel resistance. The average noise power V_{no} of an RC circuit shown in Figure 2.7 can be calculated by considering the transfer function :

$$V_{no}^2(f) = \frac{1}{1 + 4\pi^2 f^2 R^2 C^2} \times 4kTR. \quad (2.12)$$

To calculate the average voltage noise power, we have to integrate over all frequencies :

$$\overline{V_{no}^2} = \int_0^\infty \frac{4kTR}{1 + 4\pi^2 f^2 R^2 C^2} df = \frac{kT}{C}. \quad (2.13)$$

The important result is the noise power is not a function of the resistor, only the capacitor value.

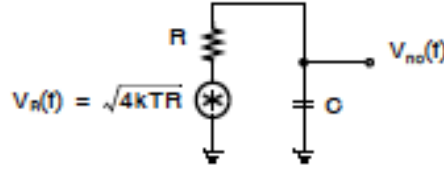


Figure 2.7: Noise of a simple RC circuit taken from [8].

The other noise source is flicker noise in MOS transistors and is related to random trapping of charges at the surface of the channel because of defects [24]. This noise can be modelled as a noise voltage source at the gate with PSD given by

$$V_n^2(f) = \frac{K}{C_{OX}WL} \times \frac{1}{f}, \quad (2.14)$$

where K is a technology dependent coefficient on the order of $10^{-25} \text{ V}^2 \cdot \text{F}$, C_{OX} is the gate oxide capacitance per unit area, and W and L are the width and length of transistor,

respectively. As this equation shows, flicker noise has high power density at low frequencies but the low frequency bound is limited because of limited time of each imaging process. At a determined bandwidth, we can estimate the integrated flicker noise by

$$\overline{V_{n_F}} = \sqrt{\frac{K}{C_{OX}WL} \ln \left(\frac{f_{high}}{f_{low}} \right)}, \quad (2.15)$$

where f_{high} and f_{low} are the upper and lower limits of integration.

The last important source of noise is shot noise. Shot noise can be defined for quantized variables like photons and electrons. For photons, the concept of shot noise can be explained with random arrival time of particles to detector. So at each small time interval the number of photons reaching the device varies a little and this cause variation at the output [4]. If there are billions of photons arriving at each time unit, this noise is very low compared with total number of photons but if there are several photons reaching the detector at each time interval then the photonic noise can cause serious limitations. This noise follows poisson random process. The same concept exists for electrons as well. Because the electrons are quantized, a flow of electrons (current) has an uncertainty in arrival time. The electronic shot noise can be modeled for any dc current as a noise current source with the following power spectral density $I_{n_{shot}}^2$:

$$I_{n_{shot}}^2(f) = 2qI_{DC}, \quad (2.16)$$

in which I_{DC} is the dc value of the current. In pixel there are different sources of electronic shot noise like diode reverse-bias current and MOS subthreshold (leakage) current.

2.2.1.2.1 Thermal noise We now would like to determine the average noise power at the pixel output. In 3T and 4T pixels, noise calculation is tricky because these systems are not linear time invariant (LTI).

The first noise component is thermal noise. Figure 2.8 shows the general model of our 4T pixel. Figure 2.9 shows the phases in one cycle of operation. To apply these calculations, each phase of operation is evaluated and the result of each is considered as an initial condition for the next one. Also, in following calculation, the duration of each phase is assumed to be long enough so we do not take the time window limit into the account. At the end, only the effect of transistor white noise is considered here and the transistors are assumed to be completely off when $V_{GS} = 0$ and modelled by a linear resistor r_{ds} when the transistor is not off. Non-linearity and charge injection effects are not considered to simplify the analysis. Also a-Se thermal noise is assumed negligible.

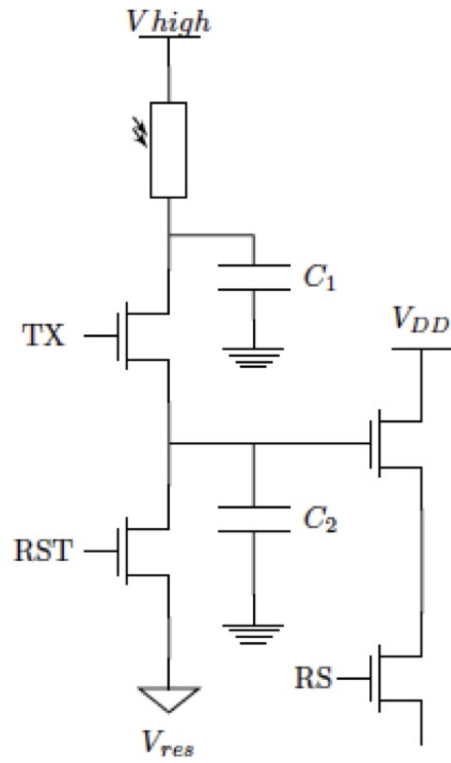


Figure 2.8: 4T Pixel with a-Se sensor.

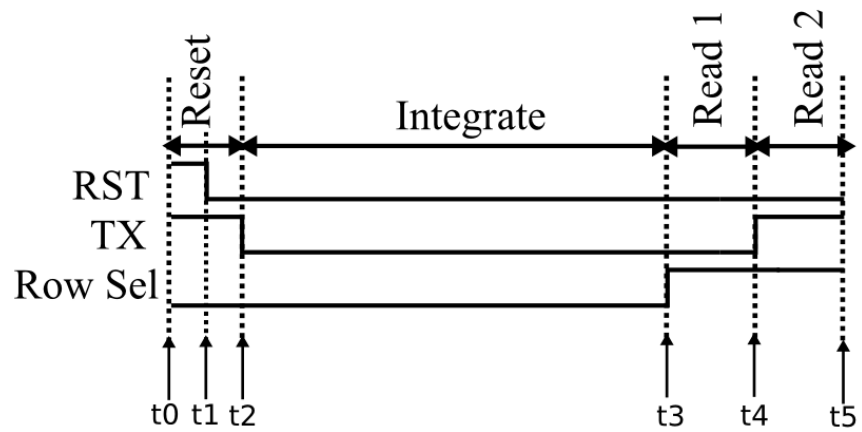


Figure 2.9: Timing of the controlling signals of one row.

Phase 1 ($t_0 < t < t_1$):

The first phase that a cycle starts with is the reset phase at time t_0 . In this phase, both transistors are on and the circuit can be modelled as in Figure 2.10. In this figure V_{n1} and V_{n2} model transistor on-resistance r_{ds} thermal noise.

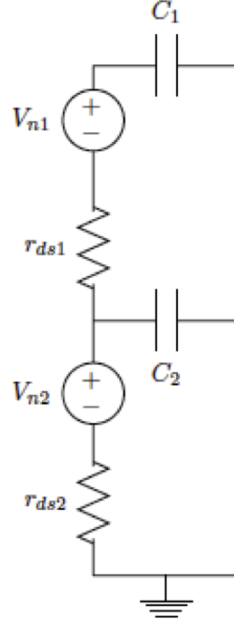


Figure 2.10: 4T pixel noise model in the reset phase.

Using superposition, the Laplace domain transfer functions between each noise source and capacitor voltages are

$$\begin{aligned}
V_{C_{22}}(s) &= \frac{R_1 C_1 s + 1}{R_1 R_2 C_1 C_2 s^2 + (R_1 C_1 + R_2 C_1 + R_2 C_2)s + 1} V_{n2}(s), \\
V_{C_{12}}(s) &= \frac{1}{R_1 R_2 C_1 C_2 s^2 + (R_1 C_1 + R_2 C_1 + R_2 C_2)s + 1} V_{n2}(s), \\
V_{C_{11}}(s) &= \frac{R_2 C_2 s + 1}{R_1 R_2 C_1 C_2 s^2 + (R_1 C_1 + R_2 C_1 + R_2 C_2)s + 1} V_{n1}(s), \\
V_{C_{21}}(s) &= \frac{-R_2 C_1 s}{R_1 R_2 C_1 C_2 s^2 + (R_1 C_1 + R_2 C_1 + R_2 C_2)s + 1} V_{n1}(s),
\end{aligned} \tag{2.17}$$

in which $V_{C_{22}}$ is the voltage across C_2 with only the V_{n2} source, $V_{C_{12}}$ is C_1 voltage in the presence of V_{n2} , $V_{C_{11}}$ is C_1 voltage in the presence of V_{n1} , and $V_{C_{21}}$ is C_2 voltage in the presence of V_{n1} . So C_1 voltage V_{C1} and C_2 voltage V_{C2} in this phase can be written as sum of two components from noise sources by superposition

$$\begin{aligned}
V_{C1}(s) &= V_{C_{11}}(s) + V_{C_{12}}(s) \\
V_{C2}(s) &= V_{C_{21}}(s) + V_{C_{22}}(s).
\end{aligned} \tag{2.18}$$

Phase 2 ($t_1 < t < t_2$):

At time t_1 , the reset transistor turns off and only TX is on. Figure 2.11 shows this situation. We use superposition to study the response due to initial stored charges on capacitors and the transistor noise source $V_n(s)$ separately. Note in this phase any charge that C_1 gets, is a discharge for C_2 . So the total charge on the capacitors will stay same and equal with the charge at the time the reset transistor turns off t_1 .

$$Q_{total} = C_1 V_{C1}(t_1) + C_2 V_{C2}(t_1) = C_1 V_{C1}(t) + C_2 V_{C2}(t) \tag{2.19}$$

Considering only the initial voltages across capacitors, the capacitor voltages are equal DC values at the steady state and can be written as

$$V_{C1_{init}} = V_{C2_{init}} = \frac{Q_{total}}{C_1 + C_2}. \tag{2.20}$$

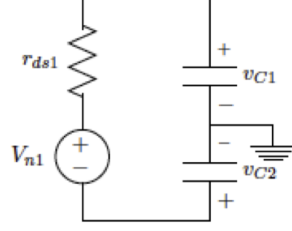


Figure 2.11: Using superposition when RST transistor is off and TX is on.

The next step is solving the circuit with the noise source without initial condition. If we name the loop current in Figure 2.11 $I(s)$, the circuit can be solved by writing KVL around this loop.

$$\begin{aligned} V_{C1n}(s) - V_{C2n}(s) + R1I(s) &= V_n(s) \\ I(s) &= \frac{V_n(s)}{R_1 + \frac{1}{sC_1} + \frac{1}{sC_2}}. \end{aligned} \quad (2.21)$$

Solving these equations for $V_{C1n}(s)$ and $V_{C2n}(s)$ gives the following results.

$$\begin{aligned} V_{C2n}(s) &= \frac{C_1 V_n(s)}{R_1 C_1 C_2 s + C_1 + C_2} \\ V_{C1n}(s) &= \frac{C_2 V_n(s)}{R_1 C_1 C_2 s + C_1 + C_2}. \end{aligned} \quad (2.22)$$

To finish the superposition we have to add the results from (2.20) and (2.22) and the result is

$$\begin{aligned} V_{C2}(s) &= \frac{Q_{total}}{C_1 + C_2} - \frac{C_1 V_n(s)}{R_1 C_1 C_2 s + C_1 + C_2} \\ V_{C1}(s) &= \frac{Q_{total}}{C_1 + C_2} + \frac{C_2 V_n(s)}{R_1 C_1 C_2 s + C_1 + C_2}. \end{aligned} \quad (2.23)$$

Note $\frac{Q_{total}}{C_1 + C_2}$ part is a DC value on capacitor but its value is random and should be considered as noise. But $V_n(s) = 4kTr_{ds1}$ has energies in all frequencies.

Phase 3 ($t_2 < t < t_3$):

After this situation both transistors are off at time t_2 which means nothing changes in the circuit. The average noise voltages on the node capacitors can be determined from phase 2 equations but it is important that this value is sampled and cannot be filtered with a low-pass filter in reading phase.

Phase 4 ($t_3 < t < t_4$):

At time t_3 , circuit is like phase 3 and both transistors are off. The first read happens in this phase. The read voltage V_{read1} is equal to average noise power on gate of source follower and it is $V_2(s)$ in (2.23):

$$V_{read1} = V_{C2}(s) = \frac{Q_{total}}{C_1 + C_2} - \frac{C_1 V_n(s)}{R_1 C_1 C_2 s + C_1 + C_2}. \quad (2.24)$$

Phase 5 ($t_4 < t < t_5$):

After integration, the TX transistor turns on to transfer the integrated charge. To focus on noise analysis we assume there is no integrated charge from the a-Se sensor. The circuit topology is like Figure ???. V_{read2} happens at this moment and the noise equation is similar to V_{read1} .

$$V_{C2}(s) = \frac{Q_{total}}{C_1 + C_2} - \frac{C_1 V_n(s)}{R_1 C_1 C_2 s + C_1 + C_2}. \quad (2.25)$$

There is an important difference between V_{read1} and V_{read2} noise equations. For V_{read2} , the second part of noise which is due to $V_n(s)$ is not a sampled as DC value. So it can be filtered with the low pass filter in the path before the ADC in the signal path. Assuming the filtration is enough, we can neglect the effect of this noise. So the average noise power on second read is

$$V_{read2} = \frac{Q_{total}}{C_1 + C_2}. \quad (2.26)$$

And at the end, to apply CDS, we have to subtract V_{read1} from V_{read2} to obtain $V_{n_{final}}$:

$$V_{n_{final}} = V_{read2} - V_{read1} = \frac{C_1 V_n(s)}{R_1 C_1 C_2 s + C_1 + C_2}. \quad (2.27)$$

We can factor $C_1 + C_2$ in the denominator:

$$V_{n_{final}} = \frac{C_1}{C_1 + C_2} \times \frac{V_n(s)}{R_1 \frac{C_1 C_2}{C_1 + C_2} s + 1}. \quad (2.28)$$

And this equation is like factor $(\frac{C_1}{C_1+C_2})$ times RC noise response with $\frac{C_1 C_2}{C_1+C_2}$ capacitance. So the total noise power would be

$$\overline{V_{n_{final}}^2} = (\frac{C_1}{C_1+C_2})^2 \times \frac{kT(C_1+C_2)}{C_1 C_2} = \frac{C_1}{C_2} \times \frac{kT}{C_1+C_2}. \quad (2.29)$$

For Q1 which have almost $C_2 = 10$ fF and $C_1 = 20$ fF, $V_{n_{final}}$ noise is equal to 525 μV_{rms} . To have a better insight about the SNR, we can assume the only source of pixel noise is thermal. So if Q_{signal} is total incoming charge from the sensor during integration then the voltage at gate of source follower would be

$$V_{\text{signal}} = \frac{Q_{\text{signal}}}{C_1+C_2}. \quad (2.30)$$

So the SNR is

$$\frac{V_{\text{signal}}^2}{\overline{V_{n_{final}}^2}} = \frac{(\frac{Q_{\text{signal}}}{C_1+C_2})^2}{\frac{C_1}{C_2} \times \frac{kT}{C_1+C_2}} = \frac{Q_{\text{signal}}^2}{kT} \frac{C_2}{C_1} \frac{1}{C_1+C_2}. \quad (2.31)$$

This equation shows the noise of a pixel is like a usual pixel noises which is $\frac{kT}{C_{\text{total}}}$ but a new factor which is $\frac{C_2}{C_1}$ is introduced in this pixel. In our design, $\frac{C_2}{C_1}$ is less than 1 for Q1 because we wanted to increase dynamic range.

Also it is interesting to study V_{read2} noise which is the normal operation without CDS. As calculated this noise is $\frac{Q_{\text{total}}}{C_1+C_2}$ in which Q_{total} is a random variable. This variable comes from (2.19) and it is not straight forward like the first part to solve this. By numerical solutions, we calculated this noise and it is very close to

$$\overline{V_{\text{read2}}^2} = \frac{Q_{\text{total}}^2}{C_1+C_2} = \frac{kT}{C_1+C_2}. \quad (2.32)$$

The value is 371 μV_{rms} (equivalent to 70 e^- rms referred to sensor output) for Q1. The SNR is

$$\frac{V_{\text{signal}}^2}{\overline{V_{\text{read2}}^2}} = \frac{(\frac{Q_{\text{signal}}}{C_1+C_2})^2}{\frac{kT}{C_1+C_2}} = \frac{Q_{\text{signal}}^2}{kT} \frac{1}{C_1+C_2}. \quad (2.33)$$

If we compare the noise power in V_{read2} and the subtracted voltage $V_{n_{final}}$, we can see lower thermal noise in the subtracted result (with CDS) in Q1. But with CDS, because other sources of noise add up for two samples, at the end the CDS does not improve the system noise performance and this is what we got from experimental results. So we consider the reading operation without CDS for noise performance calculations for all pixels.

2.2.1.2.2 Flicker Noise Based on (2.15) we can estimate the average flicker noise power for source follower transistor. For this system the flicker noise of source follower would be equal to 16 electrons referred to sensor output and is almost negligible comparing with thermal noise source.

2.2.1.2.3 Shot Noise The third component of noise for this pixel is shot noise. Because the sensor leakage is less than reverse biased diode leakages we only consider the shot noise due to the diode and transistors. The average shot noise voltage power at the end of integration phase can be written as [11]

$$\overline{V_n^2}(t_{int}) = \frac{q \times I_{DC} \times t_{int}}{C_{int}^2}. \quad (2.34)$$

in which, t_{int} is integration time. So the SNR power ratio would be

$$\frac{V_{signal}^2}{V_{n_{shot}}^2} = \frac{Q_{signal}^2}{q \times I_{DC} \times t_{int}} = \frac{N_{e_{signal}}^2}{N_{e_{leak}}}, \quad (2.35)$$

in which $N_{e_{signal}}$ is number of integrated electrons produced by the sensor and $N_{e_{leak}}$ is the number of integrated electrons because of the leakage current. The sources of shot noise are dark and photo current from the sensor and also leakages from diodes and transistors in the circuit. It is really hard to predict shot noise because it depends on diode and transistor leakage currents and the order of leakage is around femtoamperes. We measured the voltage charging slope at integration node in dark and with knowing the capacitance at that node the leakage current can be estimated. The problem is the measured charging slope is not consistent per pixel but they are at same order. For Q1, the leakage current is 6.7 fF which results in 118 e⁻ input referred noise for 336 ms integration time.

Note the above calculation is based on an estimation that the pixel leakage is a constant value. But a local feedback mechanism decreases this current over time due to diode leakage dependency on the voltage across the diode. At the very first moment after reset, the voltage across diode is maximum then in the integration phase which is long comparing with other phases the leakage current gets integrated in node capacitance and starts to bring up the voltage on integration node and decreases the voltage across diode and as a result the diode leakage decreases over time in integration phase. So we cannot expect the simple relationship of equation 2.34 between shot noise and the integration time.

Other kinds of noise are not usually main component and not a focus in this project. In our imager leakage shot noise and kTC noise both are on the same order and depending

on integration time, one of these sources can be dominant comparing with other sources. Adding shot noise and kTC noise in this pixel results in total of 733 uv_{rms} (equivalent to 137 electrons) average noise voltage.

2.2.1.3 Pixel Dynamic Range

Dynamic range is the ratio between the minimum number of electrons that the pixel can detect N_{\min} and the maximum number of electrons that it can detect N_{\max} , and is given by

$$DR = 20 \log_{10} \left(\frac{N_{\max}}{N_{\min}} \right). \quad (2.36)$$

To maximize the dynamic range, the reset voltage can be set at minimum readable voltage at the gate of the source follower transistor. The minimum reset voltage can be calculated by following equation:

$$V_{\min_{g_{SF}}} = V_{\min_{buffer}} + V_{ds_{RS}} + V_{ds_{CS}} + V_{gs_{SF}}, \quad (2.37)$$

in which $V_{\min_{buffer}}$ is the minimum input range of the buffer after the pixel and is around 0.2 V, $V_{ds_{RS}}$ and $V_{ds_{CS}}$ are voltage drops across row select and column select transistors, respectively, (but they are negligible) and $V_{gs_{SF}}$ is around 0.2 V that comes from transistor sizing and biasing current. So the minimum reset voltage is expected to be 0.4 V.

There are two mechanisms that can end the charge transfer for the circuit in Figure 2.8. First one is when the TX transistor's drain voltage drops one threshold below the gate voltage $V_{dd} - V_{th_{TX}}$ and the operation mode changes to saturation. The second possibility is that the voltages at drain and source nodes of TX transistor get equal and it stays in triode mode. To check this we assume the transistor drain and source voltages are equal. The maximum voltage, V_{\max} at gate of source follower is the total integrated charge divided by the total capacitance at both nodes:

$$V_{\max_{Q1}} = \frac{(V_{dd} + V_{th_{diode}}) \times C_1}{C_1 + C_2}, \quad (2.38)$$

in which C_1 is total capacitance at integration node (20 fF) and C_2 is the total capacitance at the other side of TX transistor (10 fF). So with this assumption, V_{\max} would be 2.8 V. This voltage is greater than $V_{dd} - V_{th_{TX}} = 2.3$ V and it is not possible to transfer this voltage to the gate of source follower. So the conclusion is that the assumption was wrong and the mechanism that stops charge transfer is that the TX transistor operates

in saturation mode and the maximum charge in that case is when C_2 voltage reaches $V_{dd} - V_{th_{TX}} = 2.3$ V.

To calculate DR, we need to calculate minimum and maximum number of electrons that the pixel can count. To calculate the maximum we have to see how many electrons result in the maximum voltage that makes both nodes voltages equal to $V_{dd} - V_{th_{TX}}$.

$$N_{max_{Q1}} = \frac{C_{total} \times (V_{dd} - V_{th_{TX}} - V_{reset})}{q}, \quad (2.39)$$

where C_{total} is the sum of capacitances at both integration node and reset node $C_1 + C_2$. When TX is on, the total capacitance is about 30 fF. Note we used C_{total} and not only the integration capacitor C_1 at integration node. The reason is for maximum charge calculation we considered the final voltage $V_{dd} - V_{th_{TX}}$ where both nodes has equal voltage. This means C_1 voltage is higher than $V_{dd} - V_{th_{TX}}$ at the end of integration phase before opening the TX gate and reduced to that value after discharging on C_2 . If the minimum reset voltage is 0.2 V (note we only consider pixel limitations and buffer input limitations are not considered for V_{reset}), this results in total of 393.8×10^3 e⁻ integrated charge.

The minimum limit of dynamic range is determined by noise of the pixel. We define the minimum acceptable SNR = 1. With this definition, the noise is the floor for dynamic range. To calculate the noise, we consider to main source of noise as described in the previous section, shot noise, and kTC noise. Also, shot noise calculation based on simulated transistor leakage is not accurate at all so we use the measured leakages as reference for this calculation. For pixels in Q1, the total calculated rms noise is 137.5 e⁻. Note this noise is dependent on integration time because of shot noise dependency on it. We consider 336 ms integration time as worst case (higher integration time results in lower DR). With this integration time the DR can be calculated as

$$DR_{Q1} = 20 \log_{10} \left(\frac{393.8 \times 10^3}{137.5} \right) = 69.1 \text{ dB}. \quad (2.40)$$

For X-ray imagers this result is considered as normal dynamic range. Teledyne DALSA XINEOS 2121 and 3131 CMOS X-ray imagers for dental and industrial applications have 74 dB and 75 dB in high dynamic range mode and 64 dB and 65 dB in low dose mode.

2.2.2 Quadrant 2

Pixels in Q2 have two MIM capacitors: one at integration node and the other at the gate of the source follower. Although the pixel architecture is 6T, pixels in Q2 are operated like

Q1 pixels. Figure 2.12 shows the schematic and Figure 2.13 shows the layout design of this pixel. Table 2.2 includes the devices information of this pixel architecture. Because we have used two MIM caps, the area is twice compared to Q1. Pixel size is $11.2 \mu\text{m} \times 6.25 \mu\text{m}$ and because we had more area for transistors, TX and RS transistors in Q1 are replaced by transmission gates which include a PMOS and NMOS in parallel. Transmission gate can pass any voltage from 0 to V_{dd} while NMOS alone can only pass 0 to $V_{dd} - V_{th}$, so the DR of the pixel can be higher. The source follower is a native transistor like Q1. Note an explicit protection diode is not necessary in this case because the PMOS transmission gate transistor has diodes from source and drain to the bulk. The reset voltage can be set to 0 V to maximize the dynamic range of the pixel, but in practice we used 0.4 V like Q1.

Component	Type	Specification
M_{TX}	NMOS	W/L = $1 \mu\text{m}/0.50 \mu\text{m}$
M_{TX0}	PMOS	W/L = $1 \mu\text{m}/0.50 \mu\text{m}$
M_{RST}	NMOS	W/L = $1 \mu\text{m}/0.35 \mu\text{m}$
M_{SF}	native NMOS	W/L = $1.20 \mu\text{m}/1.20 \mu\text{m}$
M_{RS}	NMOS	$1.2 \mu\text{m}/0.35 \mu\text{m}$
M_{RS0}	PMOS	$1 \mu\text{m}/0.30 \mu\text{m}$
C_{int}	MIM cap	Capacitance = 17.6 fF
C_{SF}	MIM cap	Capacitance = 17.6 fF

Table 2.2: Quadrant 2 pixel components and sizes.

2.2.2.1 Pixel Gain

The pixel gain G_{Q2} can be calculated exactly like Q1. Using (2.7), this gain is found to be $3.33 \times 10^{-6} \text{ V/e}^-$. The gain has decreased compared to G_{Q1} due to C_2 increment.

2.2.2.2 Pixel Noise Performance

Shot noise and thermal noise are the dominant noise sources. As was done in analyzing pixels in Q1, the total thermal noise for Q2 is 88 e^- computed using (2.32). Also the measured leakage current on this pixel is 7.86 fF. So the total integrated shot noise for this quadrant from (2.34) is 128 e^- . Adding these noise sources results in a total of 155.7 e^- .

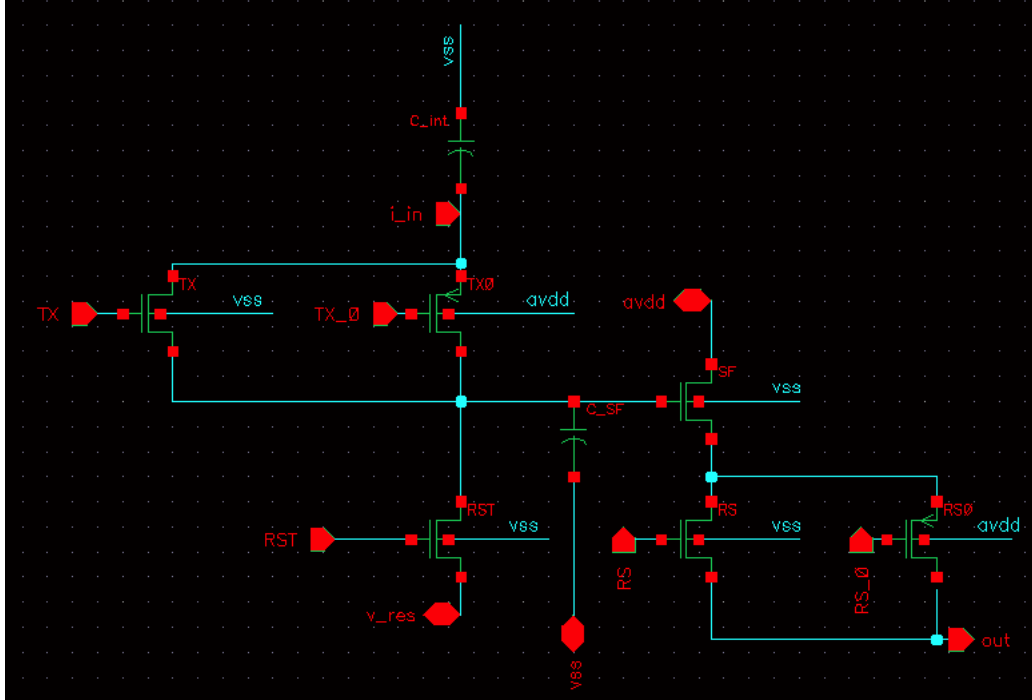


Figure 2.12: Schematic of Quadrant 2 pixel.

2.2.2.3 Pixel Dynamic Range

Because there is a full transmission gate, the maximum possible passing voltage to gate of source follower is $V_{dd} + V_{th}$ from integration node. So the charge transfer finishes when these two nodes have equal voltage (unlike pixels in Q1 which TX saturation region stops the charge transfer) so the maximum acceptable input charge is

$$N_{maxQ2} = \frac{C_1 \times (V_{dd} + V_{th} - V_{reset})}{q} = \frac{20fF \times 4.3V}{1.6 \times 10^{-19}} = 512500 \text{ e}^-. \quad (2.41)$$

The minimum signal with $SNR = 1$ has 225 input referred electrons. Now the DR can be calculated as

$$DR_{Q2} = 20 \log_{10} \left(\frac{512.5 \times 10^3}{155.7} \right) = 70.4 \text{ dB} \quad (2.42)$$

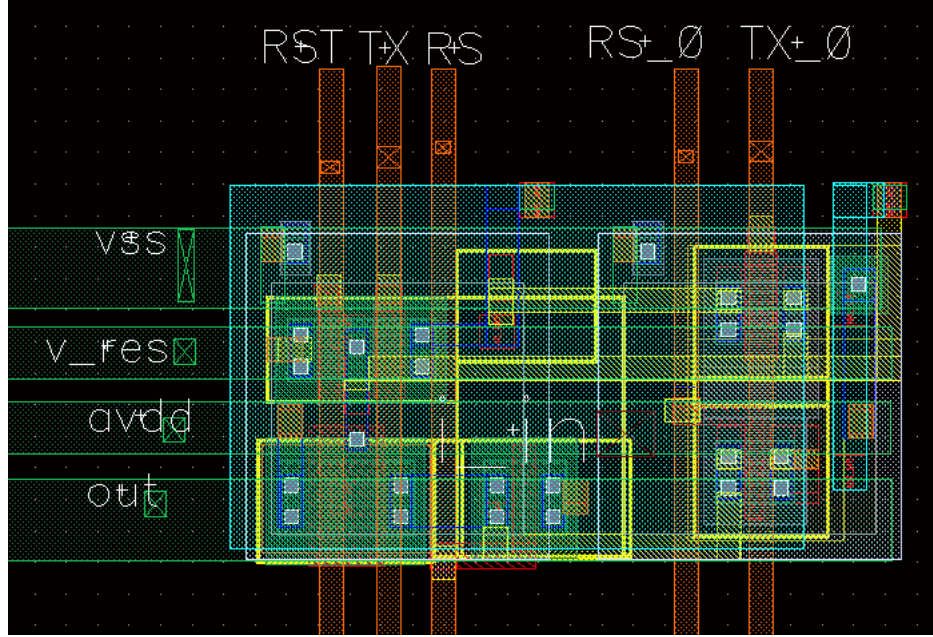


Figure 2.13: Layout of Quadrant 2 pixel.

2.2.3 Quadrant 3

Quadrant 3 contains an array of 3T pixels as a reference to compare with the response of 4T pixels. The main difference between this pixel and Q1 pixels is that the TX transistor is not used in Q3. Again, the source follower is a native transistor and an explicit protection diode is necessary. To maximize the dynamic range, the reset voltage can be set at minimum readable voltage at the gate of source follower transistor. Figure 2.14 shows the schematic and 2.15 shows the layout of one pixel with this architecture. Also the timing diagram of this pixel is shown in 2.16.

Component	Type	Specification
M_{RST}	NMOS	$W/L = 1 \mu\text{m}/0.35 \mu\text{m}$
M_{SF}	native NMOS	$W/L = 1.20 \mu\text{m}/1.20 \mu\text{m}$
M_{RS}	NMOS	$1.2 \mu\text{m}/0.35 \mu\text{m}$
D_{prot}	PN diode	$\text{Area} = 0.20 (\mu\text{m})^2$
C_{int}	MIM cap	$\text{Capacitance} = 17.6 \text{ fF}$

Table 2.3: Quadrant 3 pixel components and sizes.

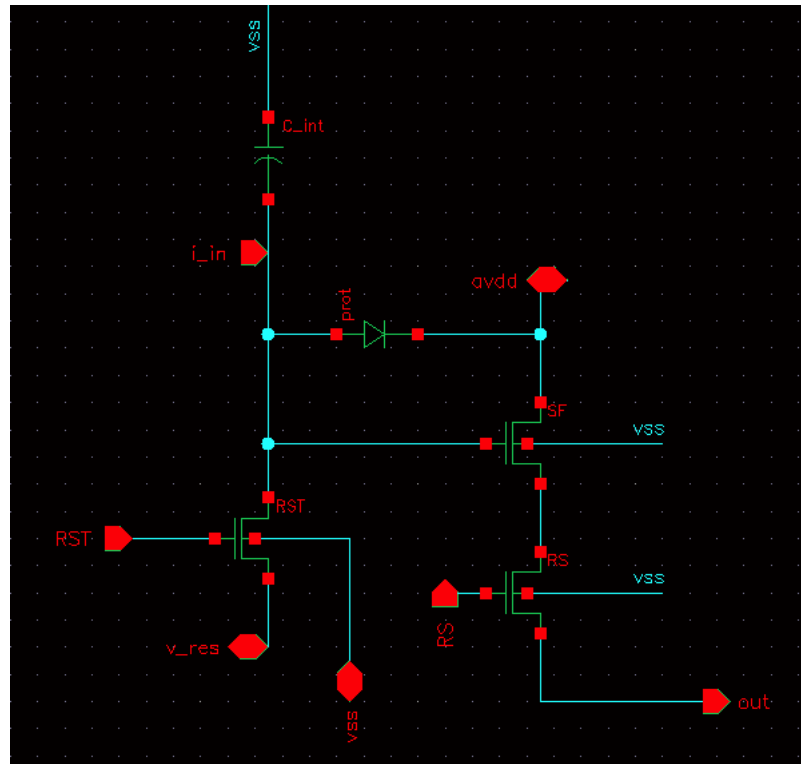


Figure 2.14: Schematic of Quadrant 3 pixel.

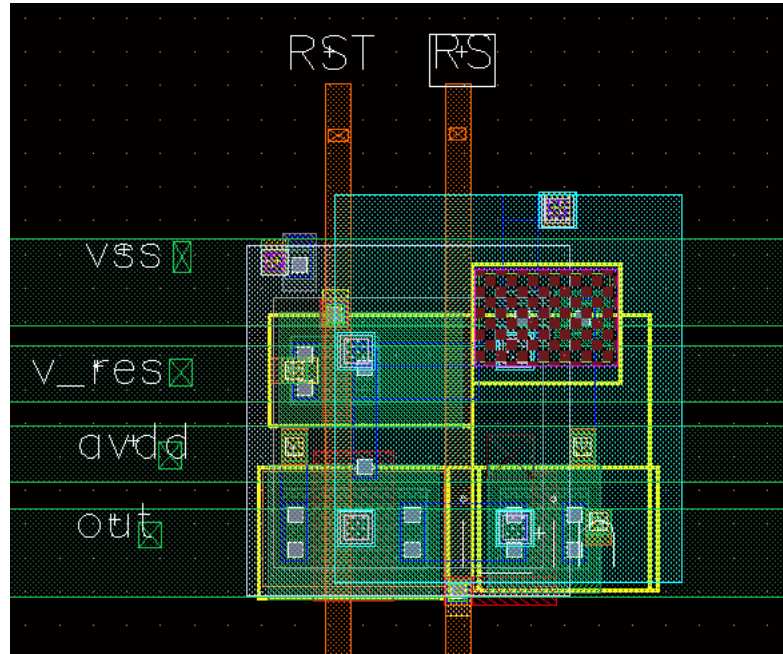


Figure 2.15: Layout of Quadrant 3 pixel.

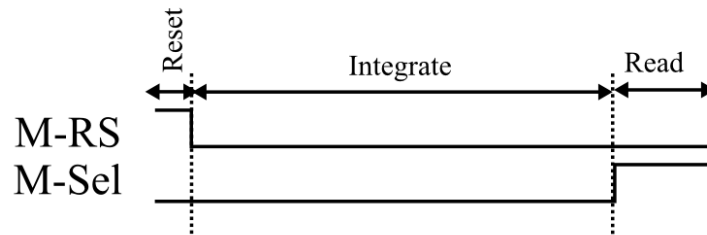


Figure 2.16: Q3 pixels timing diagram.

2.2.3.1 Pixel Gain

The pixel gain calculation is like other quadrants but lower capacitance increases the sensitivity of the pixel. The unit electron charge to voltage gain is $6.4 \times 10^{-6} \text{ V/e}^-$.

2.2.3.2 Pixel Noise Performance

Pixel noise calculation is similar to the method in 4T pixel but there is no transmission transistor. So it is straight forward to conclude from those analysis that thermal noise average voltage power is $\frac{kT}{C_{total}}$ [30]. So we can calculate it in number of equivalent electrons by

$$N_{e_{noise}} = \frac{\sqrt{kTC_{total}}}{q} = 64 \text{ e}^-. \quad (2.43)$$

In this pixel, C_{total} is equal to C_{int} plus any parasitics at integration node and is almost 25 fF. Based on the 4.2 fF measured leakage current and (2.34), the shot noise is equivalent to 94 e^- rms. Adding this noise power to shot noise for this pixel results in 114 e^- rms noise for 336 ms integration time.

2.2.3.3 Pixel Dynamic Range

The maximum voltage at integration node is $V_{dd} + V_{th_{diode}}$ but it is not transferable to output of pixel due to source follower limitation. Because the transistor is native, it can pass the voltages up to V_{dd} . So the maximum acceptable integrated charge is

$$N_{max_{Q3}} = \frac{C_{total} \times (V_{dd} - V_{reset})}{q} = \frac{25 \text{ fF} \times 3.1 \text{ V}}{1.6 \times 10^{-19}} = 484375 \text{ e}^-. \quad (2.44)$$

The minimum number of electrons is determined by the pixel noise i.e. 114 e^- . So the dynamic range in 336 ms integration is 72.57 dB.

2.2.4 Quadrant 4

Quadrant 4 uses 4T pixels but the main difference with Q1 is that no native transistor is used and the source follower is a normal transistor. Figure 2.14 shows the schematic and Figure 2.18 shows the layout of this pixel architecture. The main feature in this pixel is avoidance of a native device for the source follower. As we mentioned native transistors have weaker transconductance and the noise performance is different as well. So the voltage drop across source follower is around 1 V and some modifications are necessary for this pixel. The minimum possible output of these pixels is 0.4 V, so the minimum readable voltage at gate of source follower is V_{th} more than 0.4 V. So the reset voltage on this pixel cannot be 0.4 V like the other pixels and it should be a V_{th} more than other pixels which is around 1.4 V assuming 1 V for V_{th} .

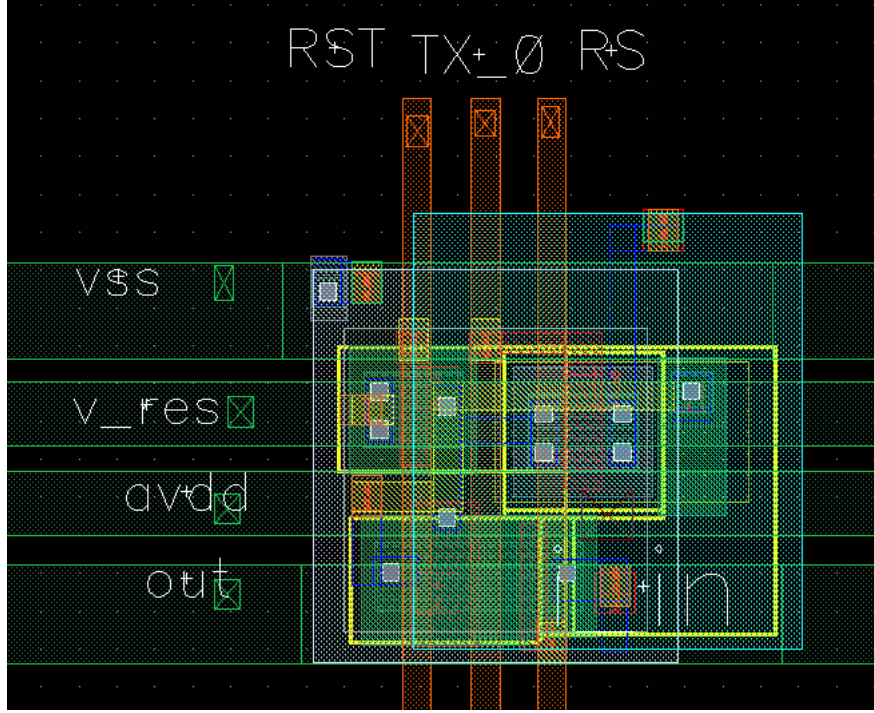


Figure 2.18: Layout of Quadrant 4 pixel.

2.2.4.1 Pixel Gain

The same method is applied for gain calculation of this quadrant. The main difference is not using a native transistor which results in lower source follower gain. The pixel gain is

$$G_{Q4} = \frac{e}{C_1 + C_2 + C_{par}} \times \frac{1}{1 + \eta} \approx \frac{1.6 \times 10^{-19} C}{30 fF} \times 0.8 = 4.27 \mu V / e^- . \quad (2.45)$$

2.2.4.2 Pixel Noise Performance

We use same method as other pixels to calculate input referred noise. The thermal noise is exactly like Q1 and is $70 e^-$ rms and the integrated shot noise of 1.25 fF leakage current for 336 ms integration is $51 e^-$ rms. The total input referred noise is $86 e^-$ rms. Note the leakage current in Q4 is less than other pixels. We believe this is due to the high reset voltage in this pixel. As shown in previous chapter, this pixel does not implemented by native transistor and the reset voltage should be one threshold higher than other pixels

reset voltage. Higher reset voltage results to less voltage across protection diode and less leakage through this device.

2.2.4.3 Pixel Dynamic Range

We need to calculate minimum and maximum input as number of electrons. The maximum is when C_1 , which is about 20 fF, is charged to $V_{dd} + V_{th}$. After voltage division the voltage at both nodes V_{final} would be

$$V_{final_{Q4}} = V_{reset} + \frac{C_1}{C_1 + C_2} \times (V_{dd} + V_{th} - V_{reset}) = 1.2V + \frac{2}{3} \times (3.3 + 1 - 1.2) = 3.27 \text{ V.} \quad (2.46)$$

Because the TX transistor is PMOS, it can pass this voltage completely and the input charge is

$$N_{max_{Q4}} = \frac{C_{int} \times (V_{dd} + V_{th} - V_{reset})}{q} = 500000 \text{ e}^-. \quad (2.47)$$

The total noise on this pixel is equal to 86 e⁻ rms. So the dynamic range is

$$DR_{Q4} = 20 \log_{10} \left(\frac{500 \times 10^3}{86} \right) = 75.3 \text{ dB.} \quad (2.48)$$

The summary of calculations for different quadrants is shown in Table 2.5. This table includes important features of each pixel design.

	Array Size	Number of Transistors	Area (μm^2)	Pixel Gain (uV/e^-)	Dynamic Range (dB)	Input Referred Noise (e^-)rms ($t_{int} = 336\text{ms}$)
Q1	32×32	4	35	5.33	69.1	137
Q2	32×32	6	70	3.33	70.4	156
Q3	32×32	3	35	6.40	72.6	114
Q4	32×32	4	35	4.27	75.3	86

Table 2.5: Pixel specifications and calculated performance summary

2.3 Digital Control Circuits

The digital circuits are necessary to operate the pixel array correctly. The row decoder in Figure 2.1 controls the TX, RST and RS signals while the column decoder controls the CS signal. Every one of these signals is composed of 64 individual nets because the imager is 64×64 .

There are total of $4 \times 64 = 256$ digital signals to control. Because it is not feasible to have I/O pad for each of these signals, we have to address them in a more efficient way. The timing that we have designed in this imager has an important feature. At each moment only one or none of these 64 signals is derived as high and the rest are low. This is true for all CS, RS, RST and TX signals and allows us to use decoders to control them. 6-to-64 decoders with an enable signal are enough to control each digital signal. With this method, the number of input pads is reduce to $4 \times 9 = 36$ for digital signals. The design of the decoders is discussed next.

2.3.1 Row Decoders

The first step is designing a 3-to-8 decoder with an enable signal. There are four inputs, three address signals (D0-D2) and one enable (\overline{EN}) to this block and eight outputs. The functionality of decoder block is as follows. If $\overline{EN} = 1$ then all outputs should be zero and if $\overline{EN} = 0$, one output should be on. We can therefore express the desired output O3 as:

$$O_3 = \overline{\overline{EN} + \overline{D_2} + D_1 + D_0}. \quad (2.49)$$

Figure 2.19 shows the architecture of this design in schematic with 8 NORs and three inverters.

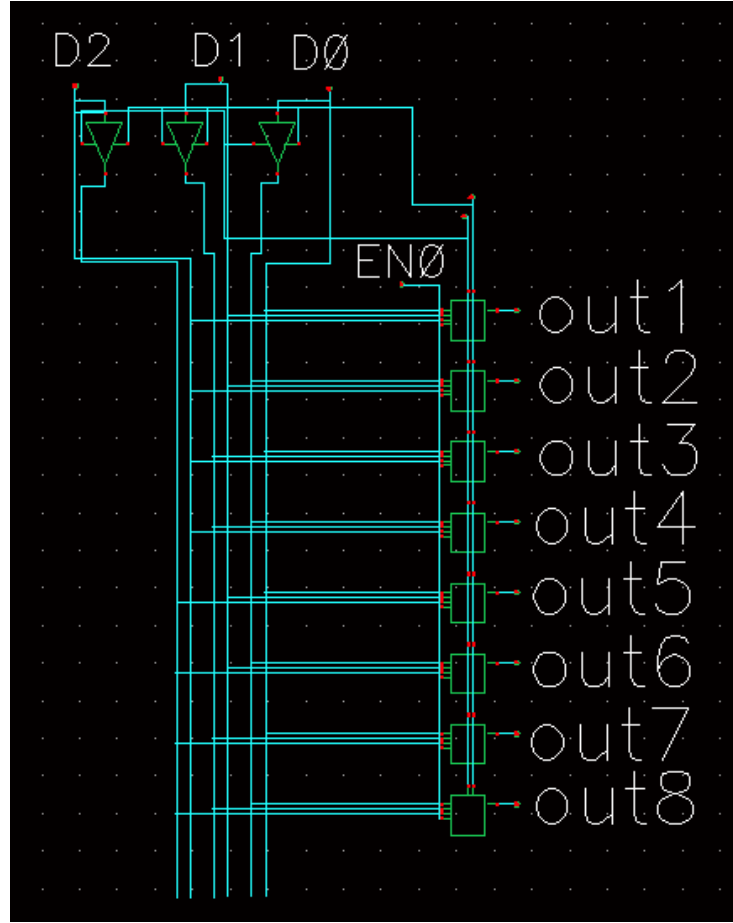


Figure 2.19: Schematic of the 3-to-8 decoder featuring enable signal. This design is based on inverters and NOR logic gates.

For implementation of the 6-to-64 decoder, nine 3-to-8 decoders and 8 inverters are used. The inputs to this block are 6 addresses, D_5 to D_0 and \overline{EN} . The first decoder has enable signal and higher address signals D_5 , D_4 and D_3 as input. Each output of this block is inverted first and then connected to \overline{EN} of one of the rest 8 decoders. Figure 2.20 shows this structure.

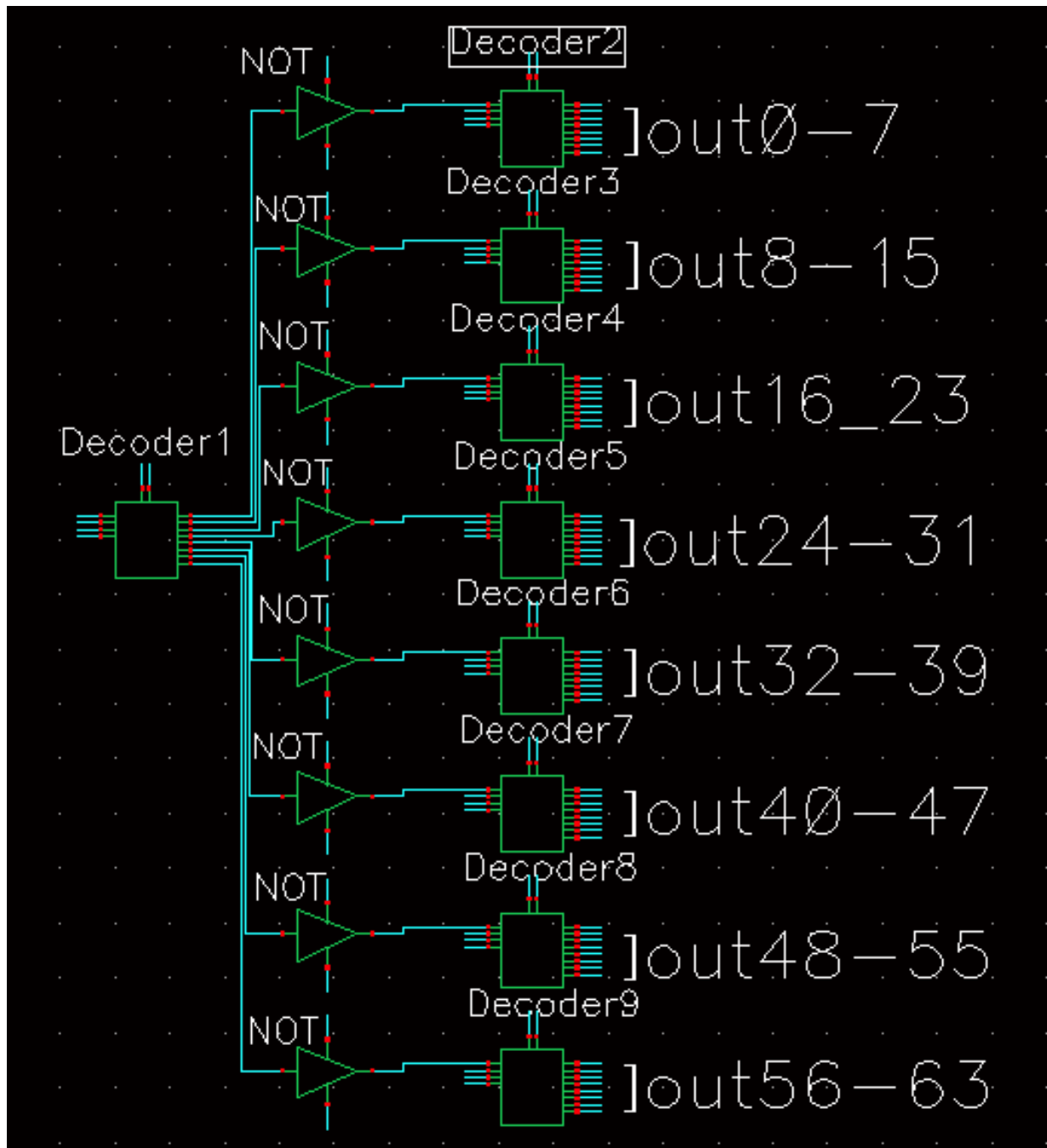


Figure 2.20: Schematic of 8-to-64 decoder.

The other 8 decoders have three same inputs D_2 , D_1 and D_0 and their enable is controlled by the first decoder. In this way, all of the 64 outputs are addressed and with enable off all of the outputs are zero. This is exactly what we mentioned before for the right timing of this system. Four 6-to-64 decoders are used for four TX, RST, RS and CS signals.

In this design, each of the decoder outputs is connected to 64 pixel transistor gates which has a gate capacitor less than 5 fF. So the total loading capacitor is less than $64 \times 5 = 320$ fF which is really small for our timing regime. Wiring capacitance might increase this load but based on TSMC documents that capacitance is very low compare to 320 fF. To estimate the circuit path speed, we consider each node as a pole made by capacitor and resistance at that node [37]. In this case, the NOR output, which has to drive 64 MOS gates is the bottleneck of this path. The resistance of this node is the output resistance of a NOR gate. The worst case output resistance R_o of the gate can be estimated using $R_o = 4R_{on}$, where R_{on} is the on-resistance of a PMOS transistor and approximately 20 k Ω . The time constant at this node is $\tau_{worst} = R_o C = 25$ ns .

This is much lower than the maximum clock period at which the system operates (500 ns minimum). Three of these decoders are used directly to address TX, RS and RST signals. The address and enable signals are derived from FPGA outside of the chip and the outputs are connected directly to RST, RS and TX signals of each row in pixel array.

2.3.2 Column Decoder

The reading system includes only one analog buffer and it does not include one buffer per column. The main reason is the buffer we have designed has wide bandwidth and can support reading the whole array alone. This reduces the FPN noise. But for each pixel read, we need to switch from pixel to the next one and this is exactly what a multiplexer does. We have 64 column outputs coming out of the array and we only want to connect one of them to the buffer input at each time. So column outputs from pixel array are input data to this multiplexer and column select signals generated from FPGA set the address of the column to be read. Figure 2.21 shows the timing of the column selection during reading of one row. As shown, when the reading phase starts the first column is selected for the first read and by the end of reading phase of the row all columns are read.

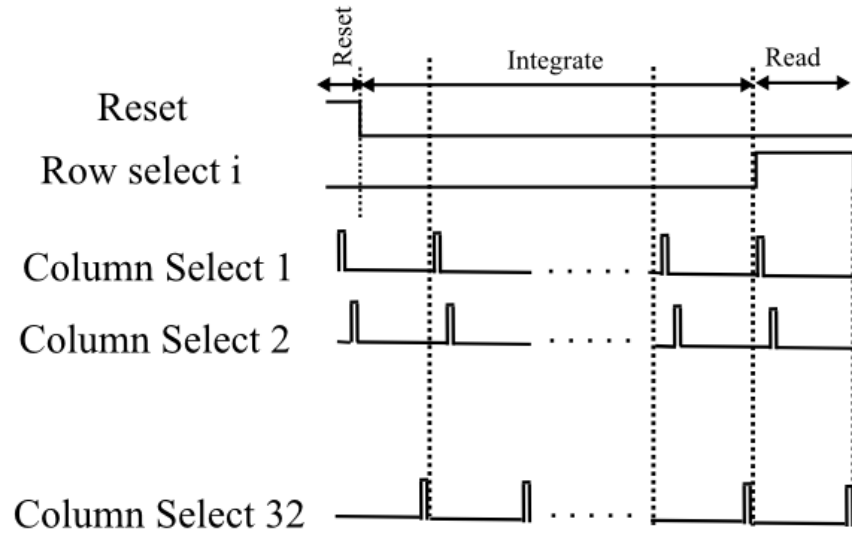


Figure 2.21: Column decoder timing for one quadrant.

To generate a 64 input multiplexer, we have used 64 transmission gates. One side of these transmission gates (including an NMOS and a PMOS) is connected to column outputs and the other side of these gates are connected to the chip output buffer. Figure 2.22 shows the schematic of this multiplexer.

margin and noise are calculated.

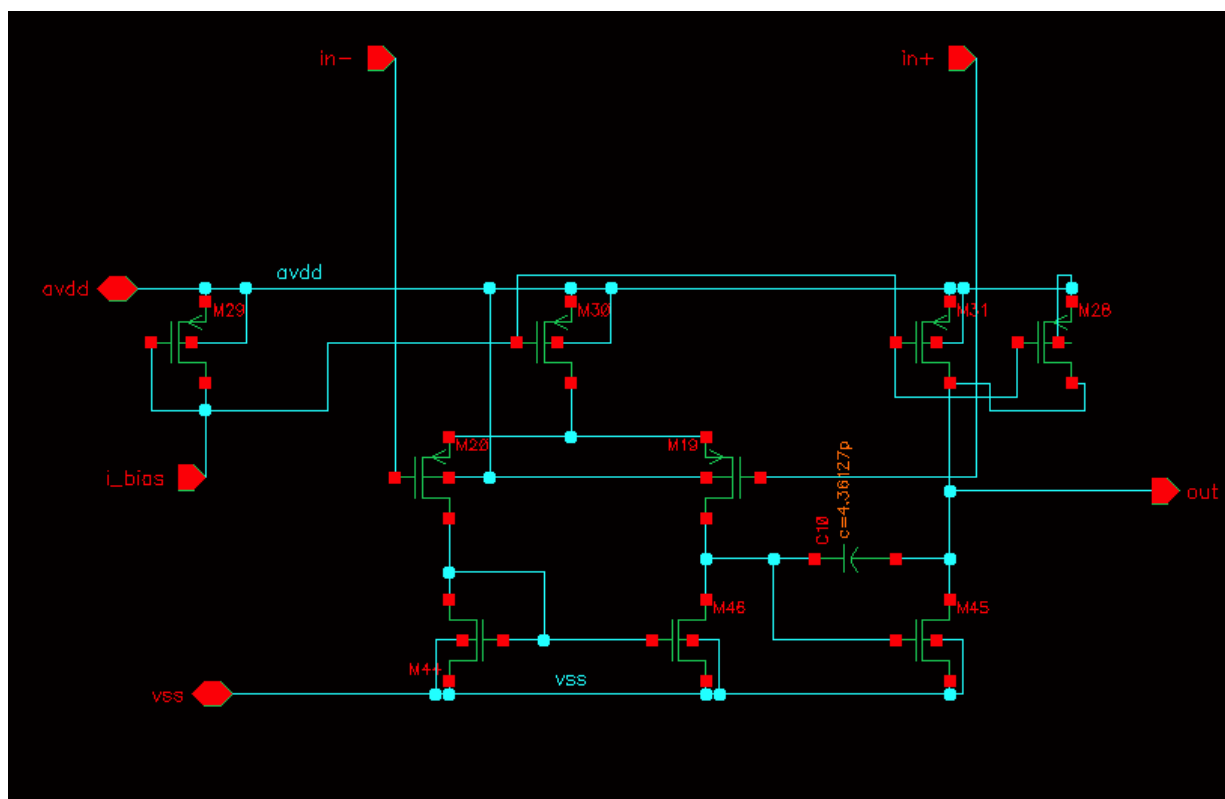


Figure 2.23: Differential amplifier used to build the on-chip output buffer.

Component	Type	Specification
M29	PMOS	W/L = 25 $\mu\text{m}/1 \mu\text{m}$
M30	PMOS	W/L = 80 $\mu\text{m}/1 \mu\text{m}$
M19	PMOS	W/L = 40 $\mu\text{m}/1 \mu\text{m}$
M20	PMOS	W/L = 40 $\mu\text{m}/1 \mu\text{m}$
M44	NMOS	W/L = 8.04 $\mu\text{m}/1 \mu\text{m}$
M46	NMOS	W/L = 8.04 $\mu\text{m}/1 \mu\text{m}$
M45	NMOS	W/L = 70 $\mu\text{m}/0.5 \mu\text{m}$
M31	PMOS	W/L = 76 $\mu\text{m}/0.4 \mu\text{m}$
M28	PMOS	W/L = 76 $\mu\text{m}/0.4 \mu\text{m}$
C10	MIM Capacitor	C = 4.3 pF

Table 2.6: Components used in on-chip buffer block

2.4.1 DC analysis

Based on the input voltage limitation of this block it is important to optimize the transistor sizes in this design. The maximum dc input voltage $V_{in_{max}}$ of this stage can be calculated as

$$V_{in_{max}} = V_{dd} - V_{gs20} - V_{OV30}, \quad (2.50)$$

in which overdrive voltage is $V_{OV} = V_{gs} - V_{th}$ and threshold voltage is almost constant so all can be done is to reduce overdrive voltage in this structure. The second stage is biased with 300 μA . The current source transistor size is $(\frac{W}{L})_{M30} = 80$ and input PMOS transistors have $(\frac{W}{L})_{M19, M20} = 40$. These high ratios and low current minimize the overdrive voltage of M_{30} and M_{20} . This is important in this design because the amplifier is not rail to rail and it limits the allowable common-mode input range.

The importance of the dc gain is the error in steady state associated with the buffer. The error E can be calculated by

$$E = V_{out_{buff}} - V_{in_{buff}} \approx \frac{1}{A_v} V_{in}, \quad (2.51)$$

where, A_v is buffer DC gain, V_{out} is buffer output voltage and V_{in} is buffer input voltage. So the maximum absolute error happens at maximum input which is 2.3 V. This error should be less than the half of the ADC least significant bit (LSB). For 14 bit resolution, the maximum acceptable error is 100 μmV assuming an ADC reference voltage of 3.3 V. So based on 2.51 the minimum acceptable gain for this system is 22.8 kV/V.

The overall gain of the amplifier can be estimated by

$$A_v = A_1 \times A_2 = G_{m1}R_{out1} \times G_{m2}R_{out2}, \quad (2.52)$$

in which G_m and R_{out} are transconductance and output resistance of each stage, respectively. To calculate this gain we need to calculate these parameters:

$$G_{m1} = g_{m19} = 416 \text{ } \mu\text{A/V}^2 \quad (2.53)$$

$$G_{m2} = g_{m45} = 3.8 \text{ mA/V}^2 \quad (2.54)$$

$$R_{out1} = r_{o46} || r_{o10}(1 + g_{m10}r_{o30}) \approx r_{o46} = 322 \text{ k}\Omega \quad (2.55)$$

$$R_{out2} = r_{o28} || r_{o31} || r_{o45} = 21.9 \text{ k}\Omega \quad (2.56)$$

So $A_v = 11.2 \text{ kV/V}$. Figure 2.24 shows the voltage transfer characteristic of the op amp. This response shows $60 \text{ } \mu\text{V}$ systematic input offset and the slope is the DC gain which is $58,000 \text{ } \frac{\text{V}}{\text{V}}$. Stage one gain is $340 \text{ } \frac{\text{V}}{\text{V}}$ and second stage has gain of $170 \text{ } \frac{\text{V}}{\text{V}}$ of the total gain. Considering the calculated acceptable minimum steady-state absolute error, this gain is sufficient.

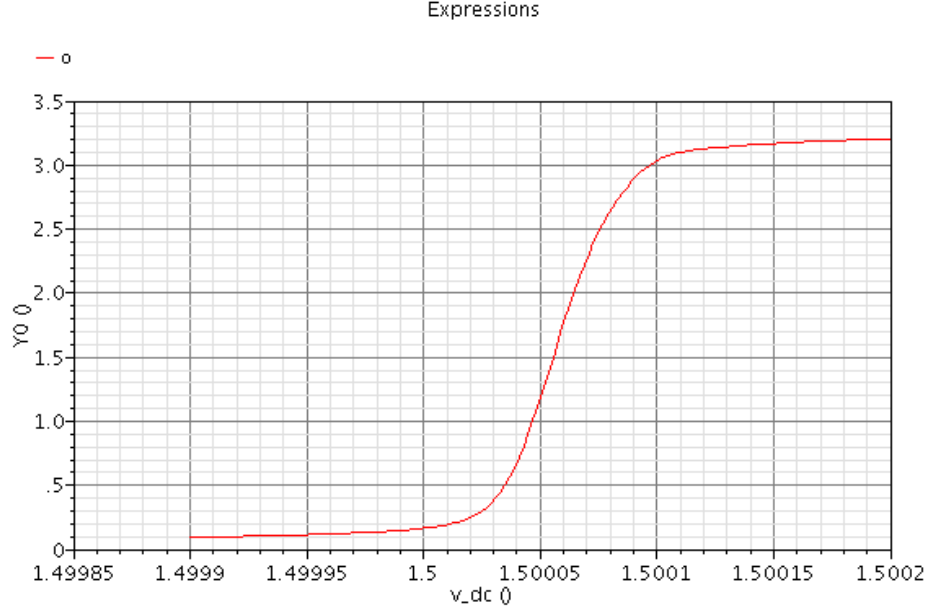


Figure 2.24: Simulated opamp voltage characteristic with negative input connected to 1.5 V.

The main reason of difference between calculated value and simulated value is that in calculations the channel-length modulation parameter λ is estimated to be 0.05 V^{-1} and 0.1 V^{-1} for NMOS and PMOS transistors respectively and this parameter determines transistor output resistances. But in the simulator this number is lower than the estimations due to dependency on transistors V_{DS} biasing voltage.

2.4.2 Frequency Response and Stability

The frequency response is important for high frame rate operation of the imager. The nature of the op amp input in this system is multiplexed-input. It means the input is not a continuous sine wave but from pixel to pixel the value changes. Because of this nature the slew rate of the op amp is important as well as the frequency response. First we discuss the frequency response and stability of this opamp.

For the maximum frame rate each pixel read has a 2 μs period. As shown in [47], for a bit resolution, settling time should be 11.09τ , where τ is the time constant. This results $\tau = 0.18 \mu\text{s}$ which is equivalent to a 3 dB bandwidth of 5.5 MHz.

In this application speed, is very important for us because the goal is 60 Hz imaging system. Stability is another issue in two stage amplifiers and needs to be addressed carefully. In frequency domain, the main factor for an amplifier is gain bandwidth product (GBP) which shows the performance of the system. We have introduced the compensation capacitor C_c from the output of stage one to output of the second stage. By Miller theorem, we can assume there is $G_2 \times C_c$ capacitance from the output of first stage to ground. The dominant pole comes from the first stage output node because of very high capacitor and resistance in respect to other nodes. So the first pole frequency would be

$$f_{pole} = \frac{1}{2\pi R_{pole} C_{pole}} = \frac{1}{2\pi R_{out1} g_{m2} R_{out2} C_c}. \quad (2.57)$$

Now GBW can be written as

$$GBW = g_{m1} g_{m2} R_{out1} R_{out2} \times \frac{1}{2\pi R_{out1} g_{m2} R_{out2} C_c} = \frac{g_{m1}}{2\pi C_c}. \quad (2.58)$$

Therefore, $GBW = 15.4 \text{ MHz}$ in our design and is sufficient because the minimum read time is 2 μs (500 kHz).

Figure 2.25 shows simulated frequency response of this block including magnitude and phase. As we can see in this plot, the gain in low frequencies is $58.1 \frac{\text{kV}}{\text{V}}$ and the 3 dB frequency is around 169 Hz. So the gain bandwidth product (GBP) is $58100 \times 169 =$

9.8 MHz which confirms the speed is high enough and it is in same order with design calculations.

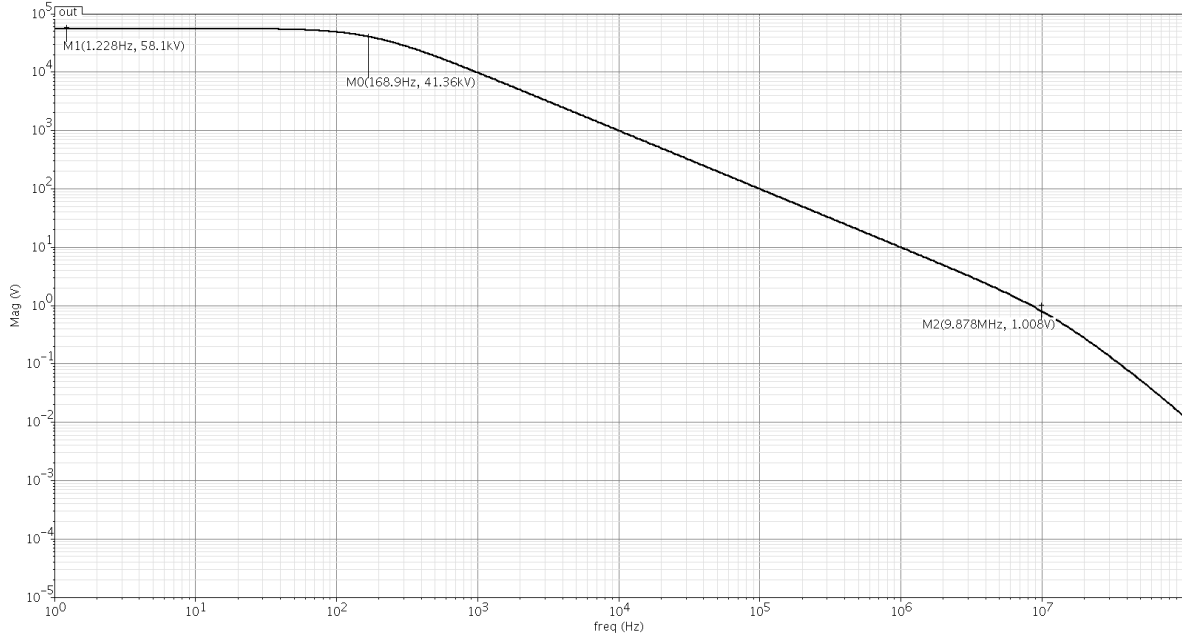


Figure 2.25: Simulated amplifier magnitude (top) response.

Stability is related to the capacitive load at the output of the op amp. As described before, the output of this opamp is connected to the input of the on board buffer so on schematic view there is very small capacitance load. If we consider the layout, because this output pin is bonded with gold wire from chip pads to the package pins and routed on PCB, at maximum load several pF capacitance is expected on this node. For safe design 50 pF capacitance is assumed to load the buffer. Figure 2.26 shows the frequency response of the opamp with this load. Phase margin (PM) is a parameter, indicating how stable is the system. In this case $PM = 55^\circ$ which is enough and no high overshoot is expected in this response. This stability is achieved using 4.36 pF capacitance for compensation technique and the stability of the on-chip buffer is guaranteed based on simulations.

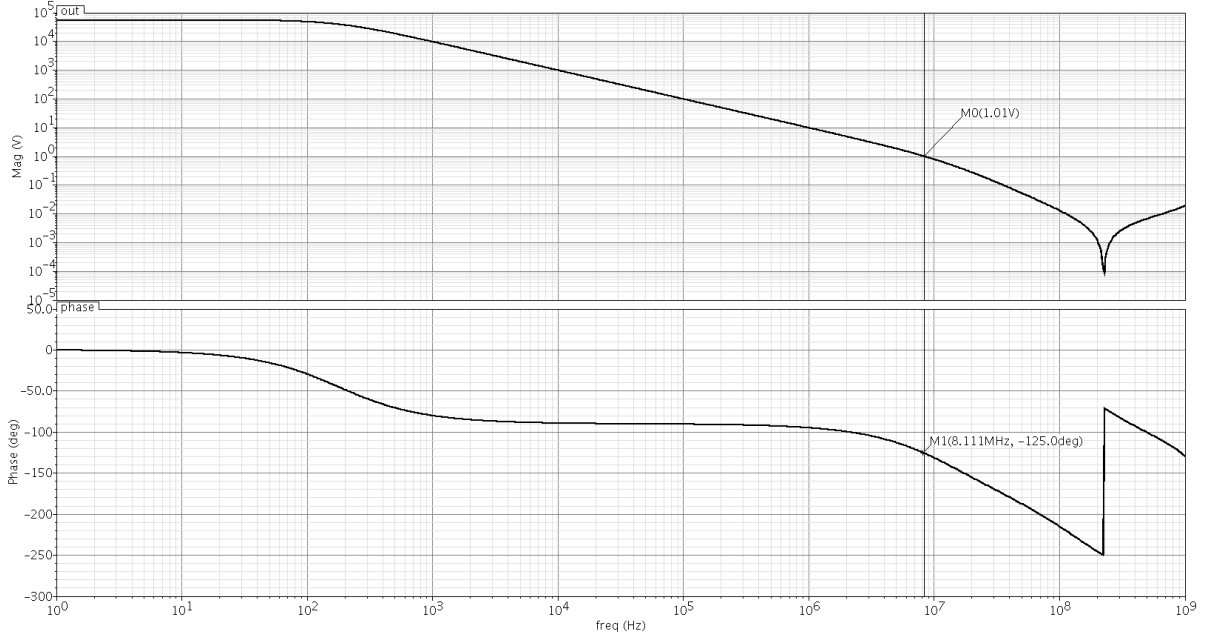


Figure 2.26: Simulated amplifier magnitude (top) and phase (bottom) response with 50 pF loading capacitance

2.4.3 Noise

Noise is important because the goal is to stay less than the pixel temporal noise. The white noise of the amplifier block usually sets by g_m of input transistors. If we decrease white noise then the flicker noise can be the limiting factor which is the case in this design. The second stage noise is not usually a concern because of gain of stage one which dominates it in noise performance. Usually the first stage is a concern because of the high gain before second stage. The input referred white noise of a differential pair with active load can be calculated as

$$V_{n_{input}}^2(f) = 2V_{n19}^2(f) + 2V_{n48}^2(f)\left(\frac{g_{m48}}{g_{m19}}\right)^2 = 2\frac{4kT\gamma}{g_{m19}} + 2\frac{4kT\gamma}{g_{m48}}\left(\frac{g_{m48}}{g_{m19}}\right)^2, \quad (2.59)$$

in which $V_n = \frac{4kT\gamma}{gm}$ for each transistor operating in saturation and γ is the excess noise factor. The total integrated noise considering the system bandwidth is equal to 25 μV_{rms} . PMOS transistors have lower flicker noise in respect to NMOS in this technology. We have chosen PMOS transistors with high W and L to decrease this noise. Based on (2.15) the

flicker noise is $30 \text{ uV}_{\text{rms}}$. So the total expected input-referred noise is $6 \text{ e}^- \text{ rms}$ which is less than 1% of the total noise power of the pixels.

Figure 2.27 shows the simulated input referred noise PSD of this amplifier. Before 100 kHz the dominant noise source is flicker noise of input transistors. The total integrated noise reported by simulator from 1Hz to 6 MHz ($\frac{\pi}{2} \times f_{\text{filter}}$ as estimation of effective passed frequency) is $60 \text{ uV}_{\text{rms}}$. The main difference between simulation and calculations is because of flicker noise that increases the total noise power at low frequencies.

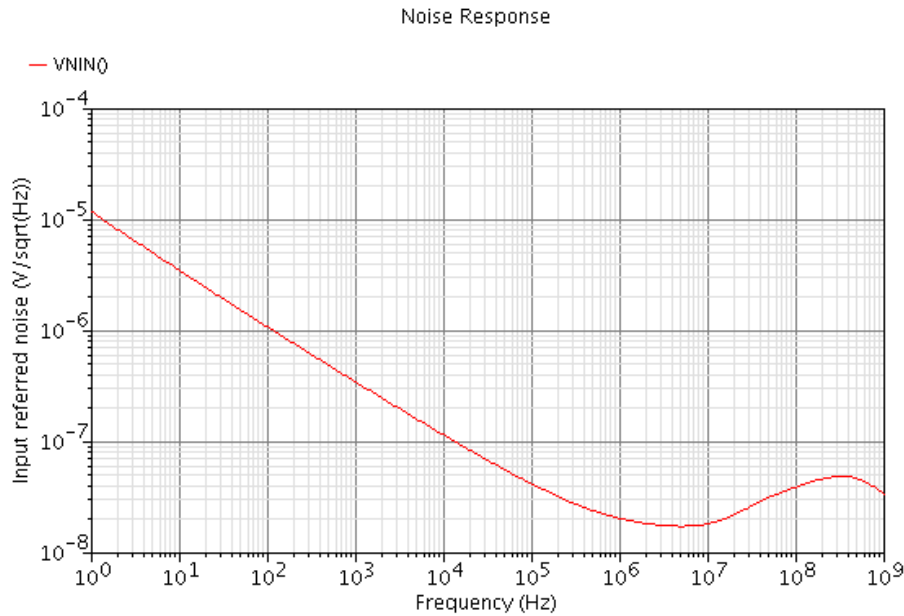


Figure 2.27: Simulated on chip buffer input referred noise versus frequency

2.4.4 Slew Rate

Slew rate of the opamp is important because of multiplexed nature of the input in this system. For the maximum operation speed, the reading period is equal to $2 / \mu\text{s}$ for each sample. We have to make sure that the slewing time for the worst case scenario is better than this period. By looking at Figure 2.23, on positive side some part of the current of pull up network of second stage charges the load capacitor. The other part passes through compensation capacitance and provides current for active load of first stage. So we can

estimate the positive slew rate, SR_{pos} with 50 pF load capacitance by

$$SR_{pos} = \frac{I_{stage2} - I_{stage1}}{C_L} = 4.8 \text{ V}/\mu\text{s}, \quad (2.60)$$

where, I_{stage1} is op amp first stage biasing current and I_{stage2} is op amp second stage biasing current. This slope is high enough because in worst case of the output has to be change from 0 to 3.3 V slewing takes almost 0.7 μs and it is smaller than 2 μs for the maximum operating speed of the system.

In negative side, because there is a gain between two sides of C_c , we can assume the input of the second stage is almost constant in respect to the other node. So the current of first stage charges up the compensation capacitance and load cap is charged separately with second stage pull down transistor. So the negative slew rate, SR_{neg} can be estimated by

$$SR_{neg} = \frac{I_{stage1}}{C_c} = 13.6 \text{ V}/\mu\text{s}. \quad (2.61)$$

Based on simulations of this block, the SR is 7.15 $\frac{\text{V}}{\mu\text{s}}$ for positive and 14.7 $\frac{\text{V}}{\mu\text{s}}$ for negative slewing.

2.5 Fabricated CMOS Chip

Figure 2.28 shows the top view of the fabricated CMOS chip before any in-house processing. These chips are not ready to use because we require a post processing step to put the a-Se sensor layer on top of the chip. Because of this post processing step, we had an important limitation that two sides of the chip had to be designed without any pads. This comes mostly from chip physical handling and placement limitations in the selenium evaporator chamber during post processing.

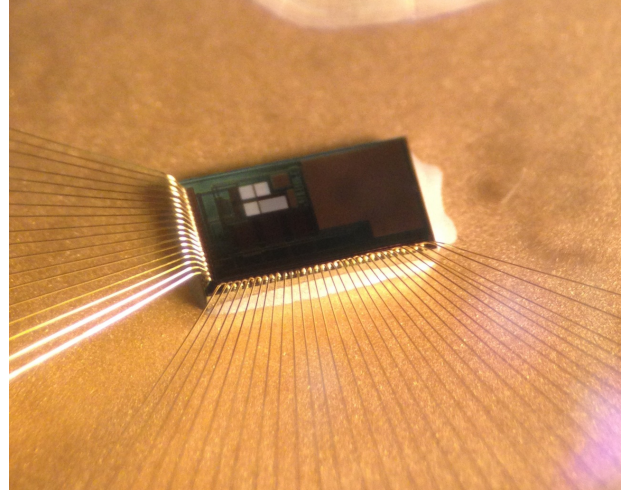
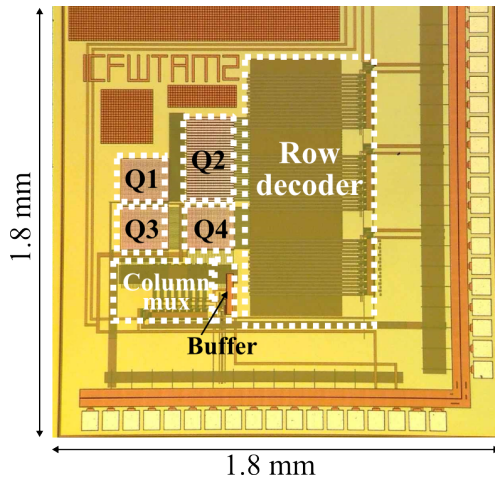


Figure 2.28: Top view of fabricated CMOS chip before post processing.

Post processing of the CMOS chip includes depositing a-Se and then the gold electrode on top of it. This is done in the G2N Lab at the University of Waterloo. The a-Se is put in a resistive boat and gets heated with electric current thorough the boat and evaporated in the chamber shown in Figure 2.30. The pixel arrays on the CMOS chip are exposed to the evaporated a-Se and under the controlled environment the a-Se gradually settles on exposed metal layer in each pixel on the CMOS chip. The parts of the CMOS chip which should not be exposed to a-Se are covered with a shadow mask during this process. Figure 2.29 shows the physical layers on top of CMOS chip. The Al cathodes are the exposed top-metal layer in each pixel.

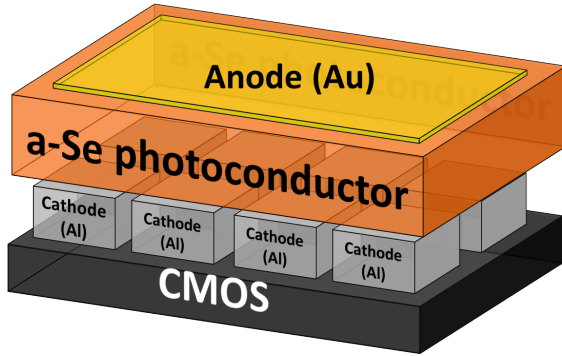


Figure 2.29: Sensor and cathode layers on top of the CMOS chip.



Figure 2.30: Selenium thermal evaporator.

The thickness of the a-Se layer can be controlled with time and temperature and it should be optimized for X-ray photon energy in each application. The thickness of a-Se is maximized based on the size of evaporation boat and in our system is $60\text{ }\mu\text{m}$. a-Se thickness between $200\text{ }\mu\text{m}$ to $500\text{ }\mu\text{m}$ is usually used for medical applications. For example, “Selenia” from Hologic uses $200\text{ }\mu\text{m}$ thickness of a-Se for direct conversion [27]. Also the thickness of gold cathode is 50 nm . Figure 2.31 shows the chip after bonding process.

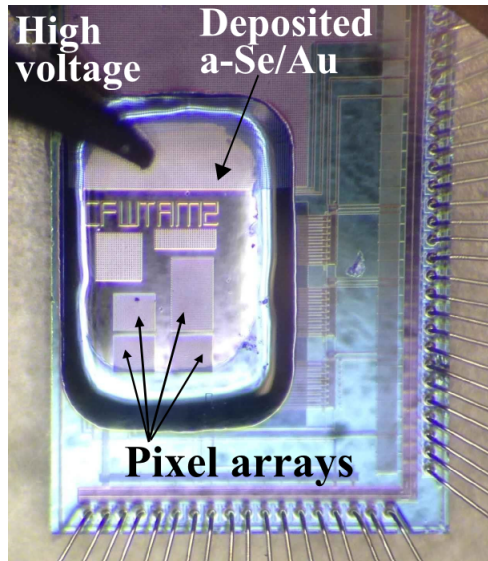


Figure 2.31: CMOS chip after bonding to package

The pad pitch on the CMOS chip is $85\text{ }\mu\text{m}$ and therefore, it is not possible to use a manual bonder. Since the material properties of a-Se can change significantly at temperatures above $60\text{ }^{\circ}\text{C}$, bonding needs to be done at lower temperatures which is unconventional. Usually ball bonder machines apply high temperatures for reliable bonding process. Prof. Michael Mayer of the Mechanical and Mechatronics Engineering Department at the University Waterloo and graduate student, Jimy Gomes, bonded our chips using a special room-temperature process that they developed.

2.6 Design of External Hardware

A custom 4-layer printed circuit board (PCB) was designed to digitally control the CMOS imager, condition and digitize the analog output from the imager, and transmit the digitized data to a PC for further processing. In addition, the PCB enabled us to mount the CMOS imager easily in an X-ray chamber while measuring its imaging performance. We now describe the main components.

2.6.1 Buffer

The buffer is built using an Analog Devices ADA4897 amplifier in unity feedback. The buffer function is to reduce loading of the on-chip buffer from other components. Based on its datasheet, the input-referred voltage noise is $1 \frac{\text{nV}}{\sqrt{\text{Hz}}}$. Over a 6 MHz bandwidth, the integrated voltage noise would be $2.45 \text{ uV}_{\text{rms}}$. So this buffer has a very low noise contribution compared to the pixel noise. Also the bandwidth is 230 MHz for unity gain feedback which is sufficient for this system.

2.6.2 Filter and ADC

The next block is a simple RC filter followed by an Analog Devices AD7980 ADC. The low pass filter prevents high frequency noise from passing to the ADC. Choosing the values for R and C needs some accurate calculations based on ADC number of bits, speed and internal capacitance [47]. As shown in this reference, to reach 16-bit settling accuracy, RC settling time of the input signal should be 11.09τ . The filter used, is close to the suggested filter in the ADC datasheet with $\tau = 50 \text{ ns}$. This is reasonable because $11.09 \times 50 \text{ ns} = 555 \text{ ns}$ and is less than the settling time in maximum speed of our imager.

The integrated noise associated with the filter is $\frac{kT}{C}$ and is less than the other thermal noises in the circuit because of the 1 nF capacitance which is high relative to other nodes. At last ADC has quantization noise which can be derived from [23]

$$V_{n_{rms}} = \frac{V_{LSB}}{\sqrt{12}}, \quad (2.62)$$

where, V_{LSB} is LSB voltage of the ADC. With a 3.3 V voltage reference and 16 bit ADC, quantization noise is $14.5 \text{ uV}_{\text{rms}}$ which is much less than the pixel noise.

2.6.3 FPGA Board

To control and manage signals and also to transfer the ADC output from the PCB to a PC, a XILINX Spartan 6 FPGA located on an Opal Kelly 6010 daughterboard is used. The Opal Kelly board is mounted on our PCB and it communicates with a PC through a USB port. Figure 2.32 shows the PCB with all FPGA daughter board mounted on it and ready to operate.

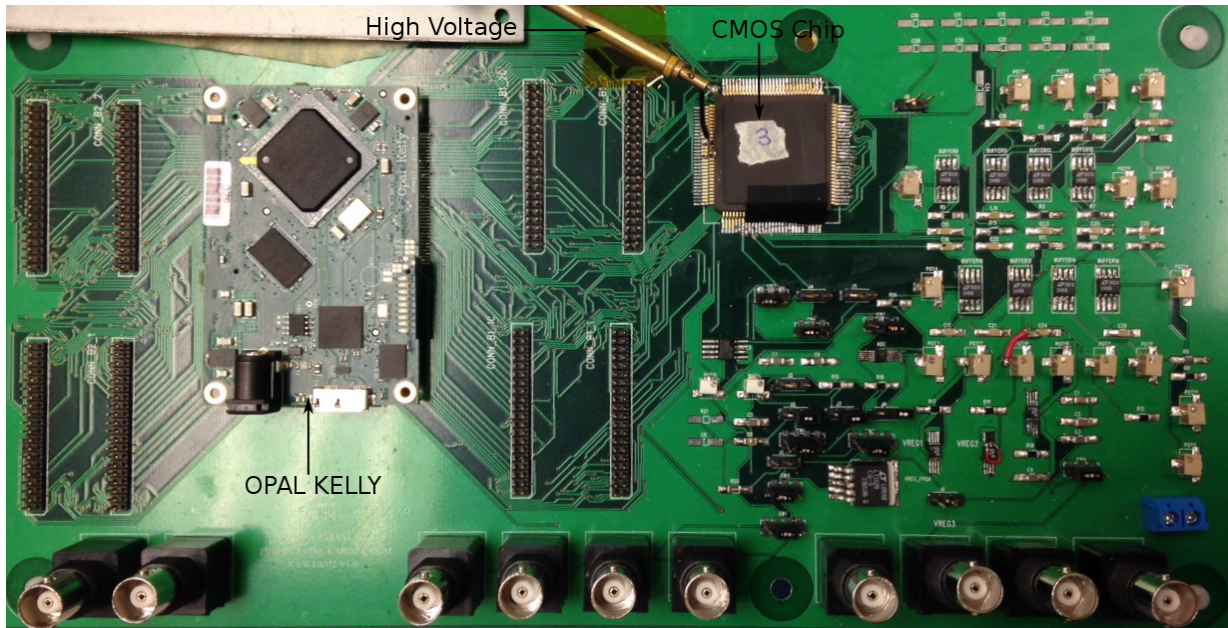


Figure 2.32: Picture of the PCB board with soldered components on it.

2.7 Control Software Design

The software includes several blocks to control, synchronize and save the data. Figure 2.33 shows the block diagram of the software system used. The main imaging controlling block is called Imager Software and the code is written in C++. This software communicates and sends the imaging information to the FPGA through a USB port and gets the read data back and saves it to memory. The other block is the “High level Controlling State Machine” which is the heart of software system and is based on hardware description language (HDL). This block get the imaging information from the Imager Software and generates synchronized controlling signals for the CMOS chip and ADC and these signals and sends the data back to imager software. CMOS Digital Signal Controller provides necessary signals for CMOS chip and ADC Controlling State Machine handles the ADC communication protocol and takes the digital data from the ADC. These two blocks are written in Verilog HDL.

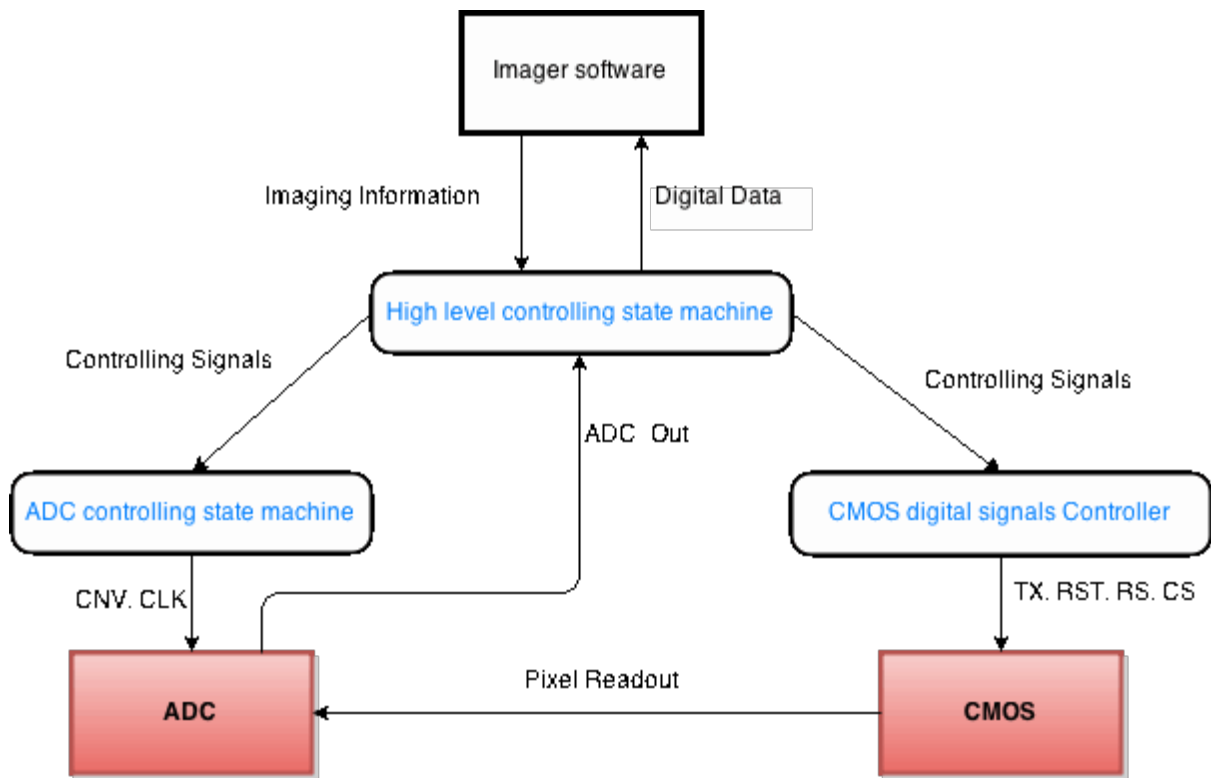


Figure 2.33: Imaging system software block diagram.

The ADC has several modes that can operate in. The mode that this system is based on is called “3-wire without busy indicator”. In this mode the rising edge of CNV pin starts the conversion and the falling edge starts the ADC_out serial data appears on output pin 1 bit per clock.

ADC Controlling State Machine is based on a Mealy state machine and beside it there are several small blocks to complete the whole system. This state machine uses Clk, Fire and ADC_out as inputs and the outputs are Out, Read_done and CNV. Clock is FPGA system clock to synchronize with other blocks as a timing reference. Fire is a signal that another state machine sends to this machine to start sampling 1 value and ADC_out is the output pin of the ADC that should be sampled. Figure 2.34 shows this state machine with 3 states. In the idle state no conversion and data sampling is happening and the ADC is waiting for a Fire signal to start sampling. Fire signal, which is controlled by another state, change the state to Converting. In this state the CNV pin of ADC stays at high and the system stays in this system so that the input signal of ADC has enough time to settle. When CNV_counter reaches to certain value the machine goes to next state which is Reading. In this state the ADC pin data is stored in a memory block. After 16 clocks the 16 bits of ADC are ready to transfer to memory block a flag called Read_done turns to 1 that informs the other state machine the 16 bit data is stored in register and ready to use. Then the state machine goes back to idle state waiting for the next Fire signal.

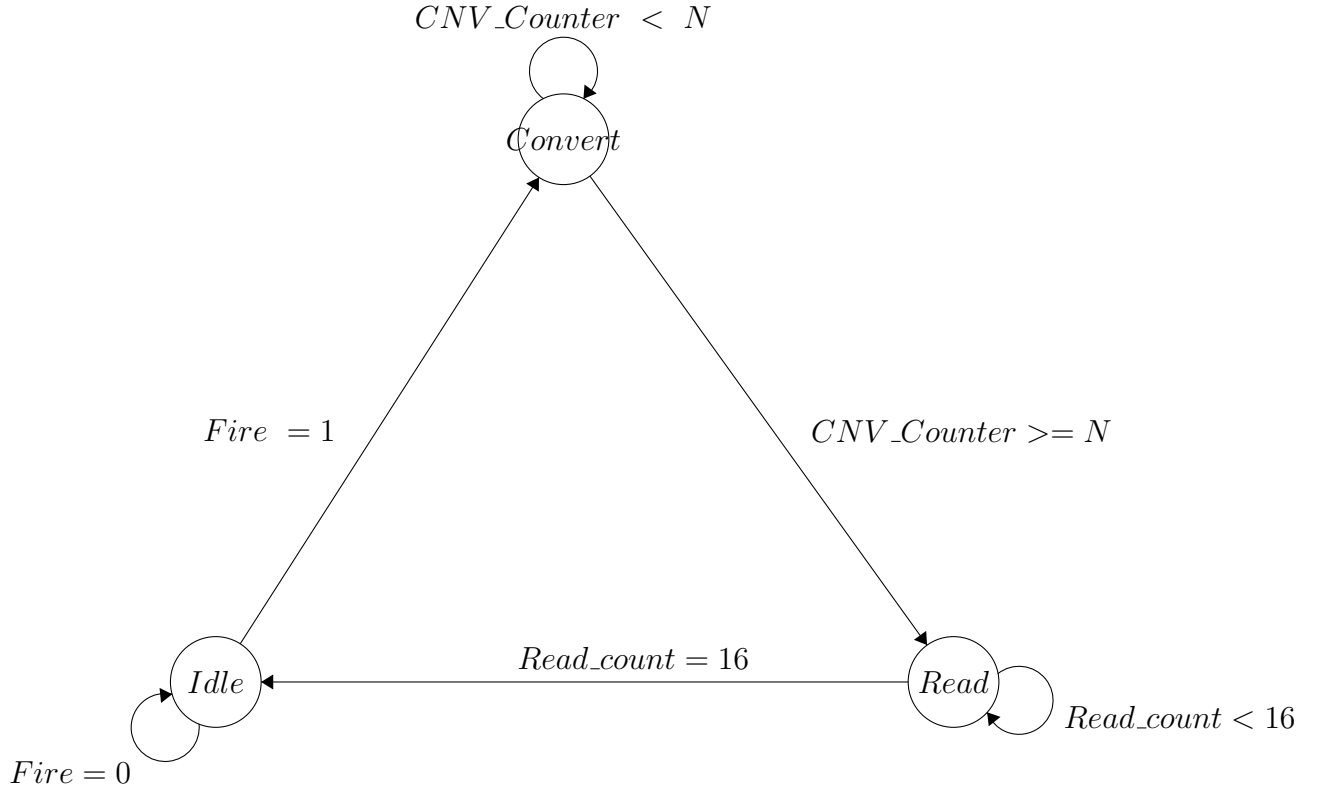


Figure 2.34: Mealy State machine to capture one sample from ADC

The other part of the controlling software is CMOS Digital Signals Controller. The duty of this block is to generate TX, RST, RS and CS signals for CMOS chip, synchronized with ADC controlling state machine. As described before the first phase is reset and there are integration and reading phase after that. The timing of this system is designed in a way that for each row one phase is happening at each moment which means the controller, controls these signals in a parallel way. So when a reading is happening for one row other rows are in integrating or resetting phase. Now with some calculations we can see the timing of each phase.

To find the interval for each phase we need to choose the reading time for each pixel. The minimum reading time that we defined for this imager is 2 us per read. With this number we can calculate the other phase. Total time per each frame is reading time of whole pixels. We have 64 by 64 array and because of CDS each pixel should be read twice.

$$T_{frame} = N_{read} \times T_{read} = 64 \times 64 \times 2 \times 2\mu s = 16.384 \text{ ms.} \quad (2.63)$$

This is the reading time of 1 frame which corresponds to 61.035 frames per second. So any node in path of the signal needs to be faster than 500 kHz. Now we can calculate the timing of each phase in Figure 2.9. Read 1 and Read 2 phases both include reading of a row. This is equal to $64 \times 2 \mu s = 128 \mu s$. The total of reset and integration phase is equal to $16384 \mu s - 256 \mu s = 16128 \mu s$. We have assigned 8 μs for reset and 16120 μs for integration. These numbers can change depending on application. Knowing the timing for each row of pixel now the FPGA can derive these signals with a way we designed it.

The High Level Controlling State Machine has manages the other two blocks we mentioned and operate them in right way. At the end, this block initiates some functions from Opal Kelly libraries to transfer the final data from the RAM on the board through USB board and this lets us to save a data on hard disc memory for later post processing and displaying the image.

Chapter 3

Experimental Results

In this chapter, the experimental results based on the implemented hardware are explained. We demonstrate that the designed system operates completely as an imager and X-ray images obtained with this imager are shown at the end of the chapter.

3.1 Experimental Setup

To obtain X-ray images with our system, we designed an experimental setup in the G2N Lab. The costume PCB containing the a-Se/CMOS imager is placed inside a lead chamber containing an X-ray source. A USB cable and imager power cables are passed thorough safe holes from the back of the chamber and connected to a PC and power supply outside the chamber. The total PCB current drawn from power supply is 32 mA at 8 V supply which results in 256 mW static power consumption. The FPGA power supply is separated and the consumption varies with speed of operation.

The X-ray source is a stationary anode mobile X-ray tungsten source with 15-mA tube current, 15° anode angle, and 3.6-mm effective Al filtration. The X-ray illumination area is adjustable and we focused it only on the CMOS chip to prevent any possible effect from the X-rays striking other components in the system. An object to be imaged is placed and fixed on top of the CMOS chip. One of the imaging difficulties was to place an interesting portion of the object on top of the small sensitive part of the CMOS imager. Figure 3.1 shows the setup for experimental measurements in which the imager board is placed inside of an X-ray chamber and it is connected to other system components.

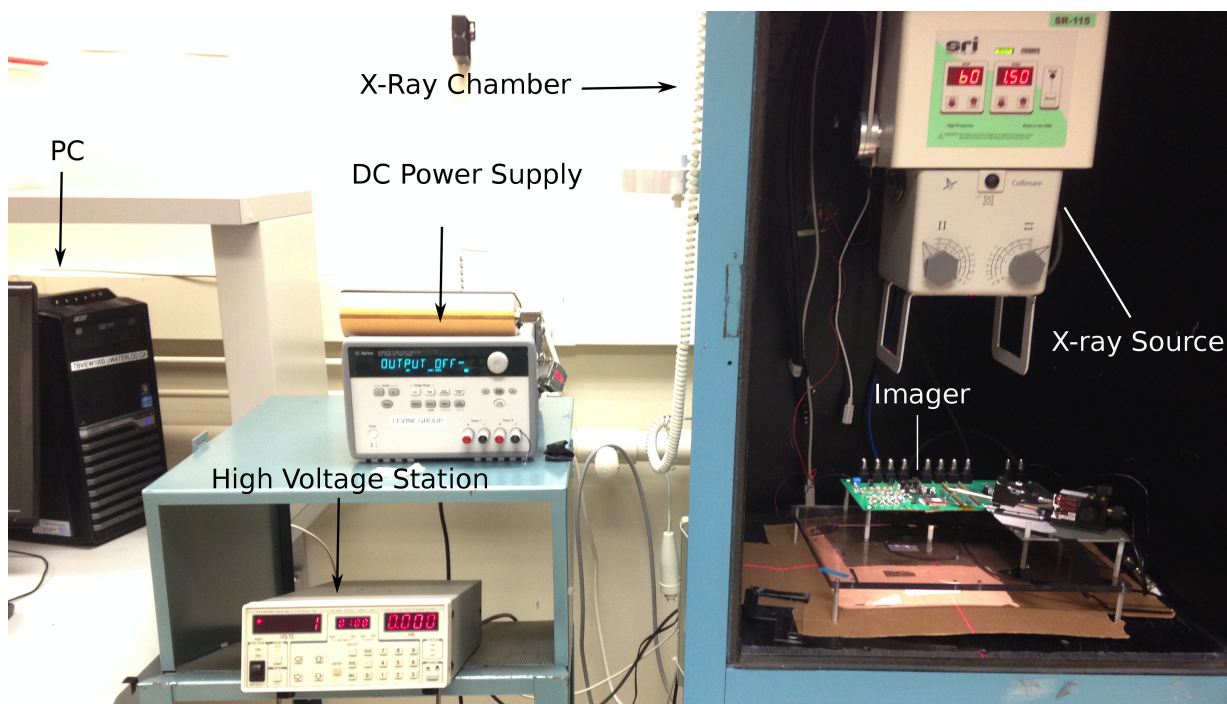


Figure 3.1: Imaging system setup for experimental measurements

3.2 Imaging Performance

3.2.1 Imager Linearity

One important performance factor of any imager is linearity. This feature is important especially if the imager is used in applications which use the data for calculations as a reference and not only visualization of an object. Any dependency of imager gain on the input value results in nonlinearity.

An experiment is done to show the linearity of the X-ray imager. Fig 3.2 shows the measured response of the imager as a function of pixel integration time when stimulated with polychromatic X-ray photons generated by a stationary anode mobile X-ray tungsten source with 50-kVp tube potential, 15-mA tube current. The average output voltage from all pixels in the array minus the offset in the dark, excluding those in the first and last row and column (calculated using the output from each pixel averaged over at most twenty consecutive frames), is linear over an integration period extending from 40 ms to 2.0 s. Changing the integration time of the imager is equal to changing the number of photons coming into the imager. Also the reason for averaging a pixel value for several frames is to decrease the noise power so that we only get the linearity response of the imager. In this figure the R-squared value of the best-fit line is calculated as well which is a factor to show how linear the data is.

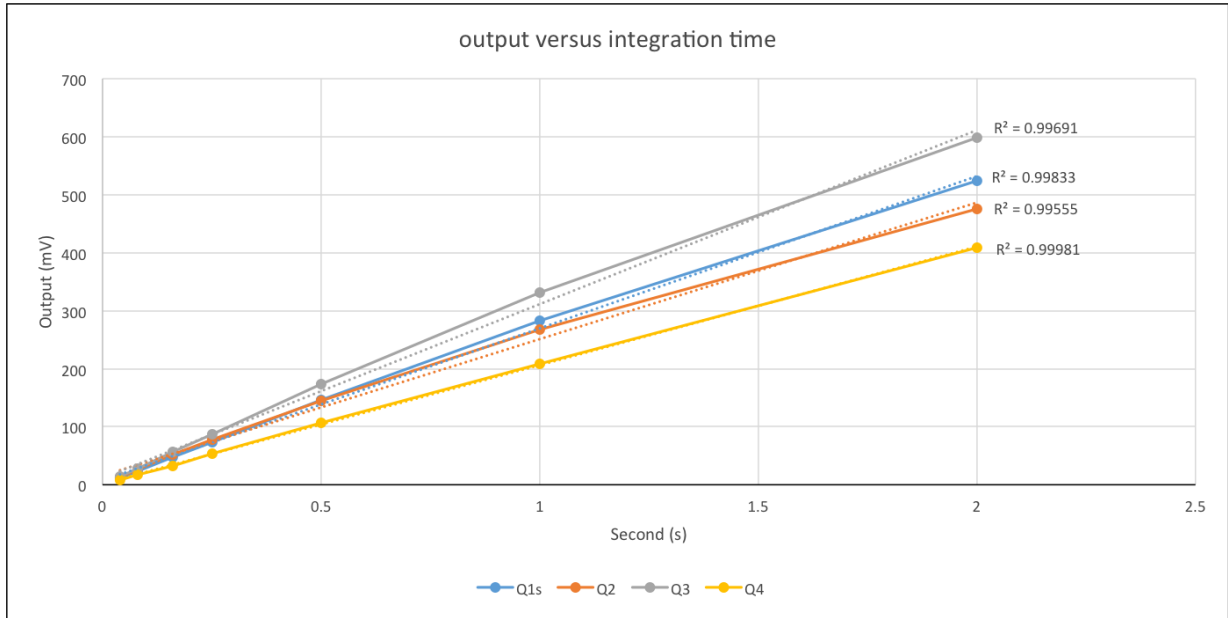


Figure 3.2: Average output from each array versus integration time of the imager while X-ray beam is on. The outputs are offset corrected with dark measurements. R-squared values of the best-fit line to each response are also included.

3.2.2 Temporal Noise Measurements

Temporal noise measurements are made by taking frames with the designed imager and studying the characteristics of the output. If we monitor the output of one pixel, a random variation can be observed. Instead of probing the output of all pixels continuously, which is not practical, we can capture enough number of images which means we sample the output of each pixel. In this case, the number of samples is number of taken images. Now consider the set of data containing the samples from one pixel. The standard deviation (SD) of these samples is the output referred noise of the whole chain in the imager for that pixel.

3.2.2.1 Temporal Noise Measurements in Dark

Figure 3.3 shows the median temporal noise in the dark for each quadrant. At each integration time, 400 frames are taken and the standard deviation is computed from these 400 values. After, the median of these standard deviations of 30×30 pixels is chosen. We use the median instead of the mean because several pixels in each quadrant are orders of magnitude away from the others and this can seriously affect the mean. We are still investigating the cause of this.

The general trend is noise increment with integration time. The average shot noise power has a linear relationship with integration time (assuming the leakage current is consistent) so the shot noise rms voltage has a square root relationship with time. In Figure 3.3, we can see the slope decreases with increasing integration time which agrees with square root response.

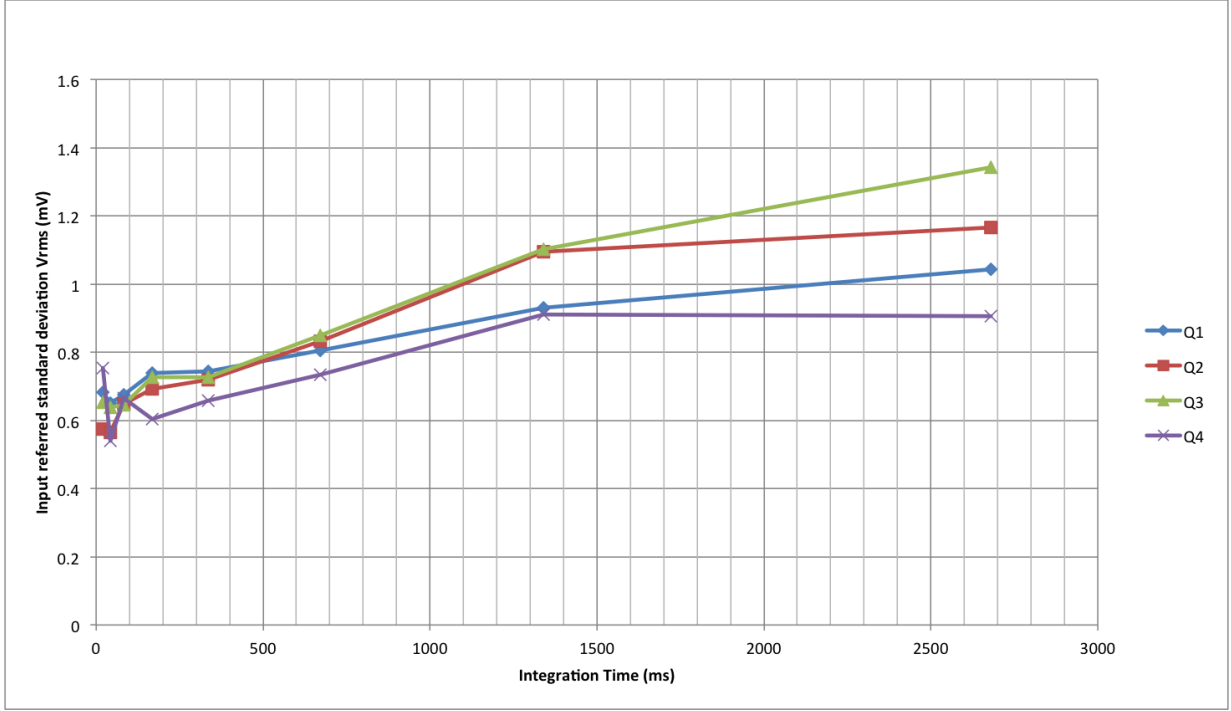


Figure 3.3: Median input-referred temporal noise in dark versus integration time for all quadrants.

Figure 3.4 shows the comparison between Q1 and Q3 based on experimental and analytical results. For acceptable comparison the noise is input referred to output of the a-Se sensor as number of electrons. Both plots show 3T pixel has better noise performance in this chip for all practical integration times.

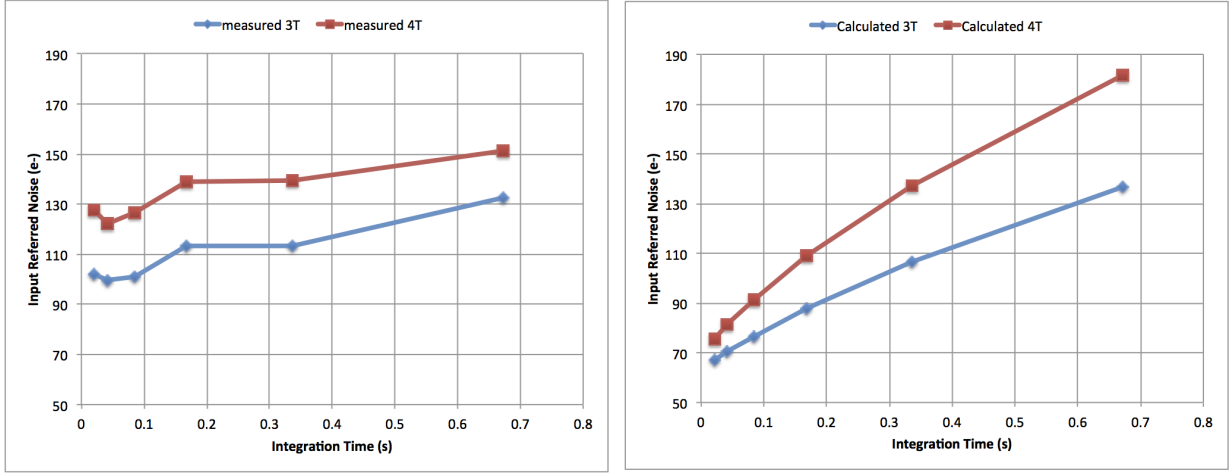


Figure 3.4: Analytical (right) and experimental (left) input-referred noise versus integration time for plots in Q1 and Q3.

3.2.2.2 Temporal Noise Measurements with X-ray

Figures 3.5, 3.6, 3.7, and 3.8 show the measured noise results for four quadrants when the X-ray is on, which includes total noise including quantum noise and readout noise. The X-ray source is same as explained in linearity measurements. Note the off chip filter before the ADC was bypassed for this data set and the flat field correction which is offset and gain correction of the images is applied to this data set. In these plots we can see the X-ray responses that are the averaged of increment of pixel output comparing to dark condition, which means the signal containing information. Based on our analysis in Chapter 2 we know the leakage shot noise increases with integration time. In the presence of X-ray, uncertainty in a-Se current caused by photon shot noise increases with integration time as well. So our expectation matches with the plots and the temporal noise increases with integration time.

3.2.3 Fixed Pattern Noise Measurement

The fixed pattern noise is different from the temporal noise explained in previous section. As opposed to temporal noise, the FPN is only a function of the spatial domain. It means this parameter is not a random variable changing with time so it cannot be categorized as electronic noise. The sources of FPN are all sources of response differences between

different pixels. For example, the source follower threshold voltage is not same for each pixel and this difference leads to offset variation which is a component of FPN.

In an ideal case of no FPN in the system, the standard deviation of all pixel responses in one image should be equal to the temporal noise of the array. But when there are variations over the array, the measured standard deviation is different. To measure FPN, 400 images in dark are taken and the output of each pixel is averaged between these frames so the temporal noise contribution reduced. The standard deviation of all averaged pixel values (which does not contain temporal noise) is the FPN of the array. Because the whole sensor dark current around the arrays flows into edge pixels, we ignored those pixels in this calculation like temporal noise.

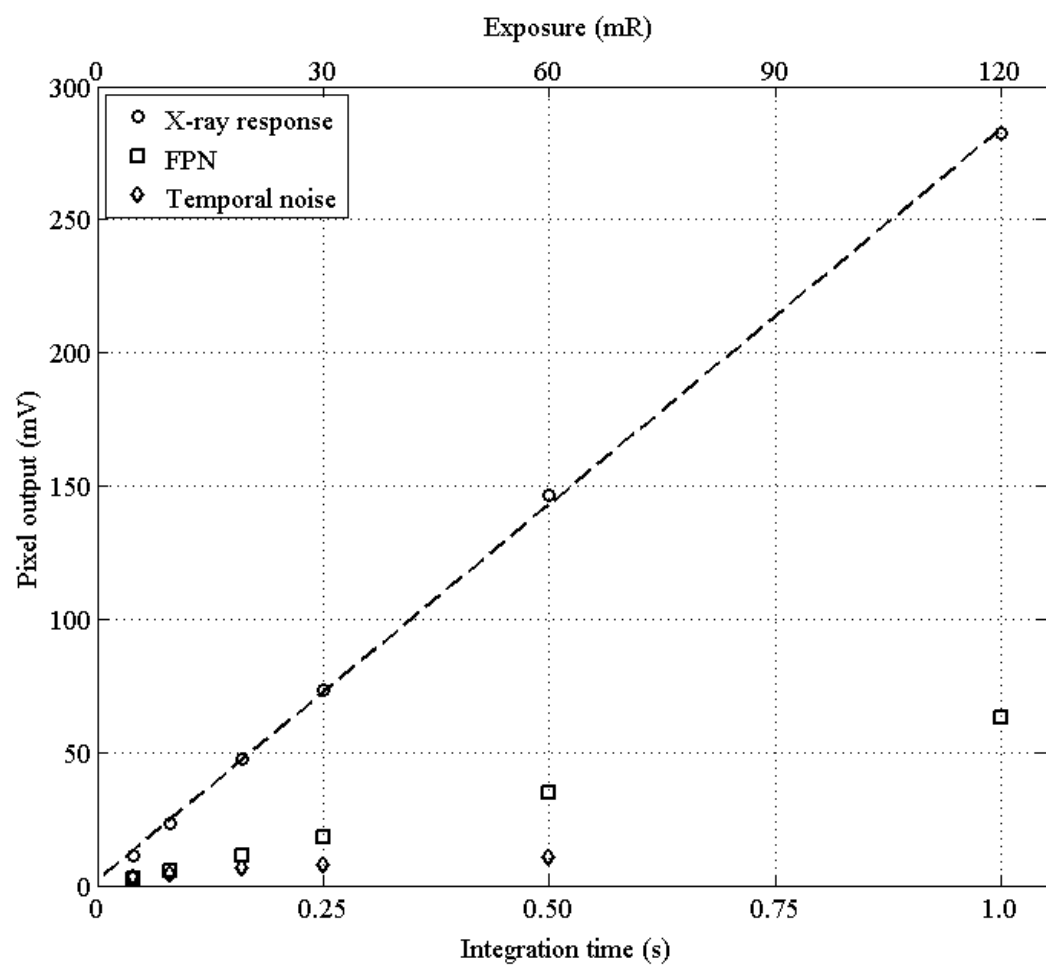


Figure 3.5: Quadrant 1 response versus integration time for all quadrants after flat field correction.

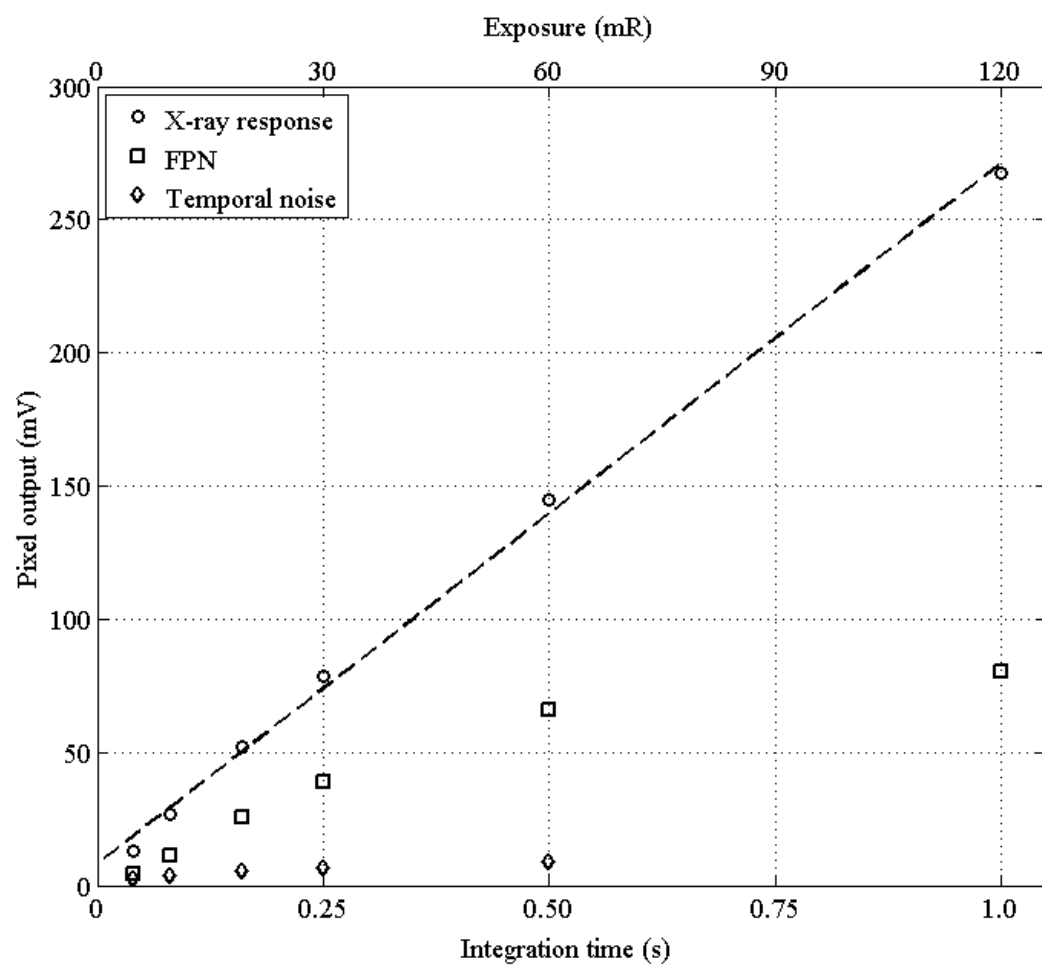


Figure 3.6: Quadrant 2 response versus integration time for all quadrants after flat field correction.

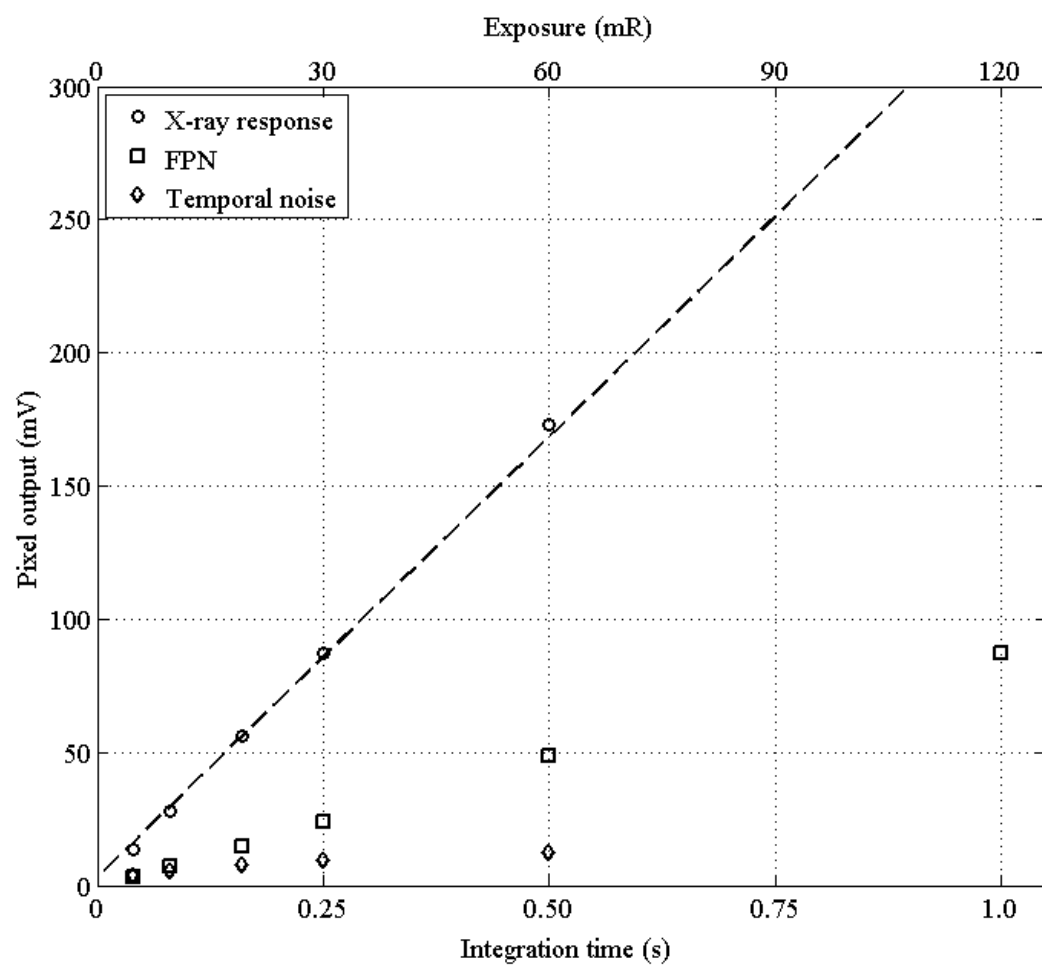


Figure 3.7: Quadrant 3 response versus integration time for all quadrants after flat field correction.

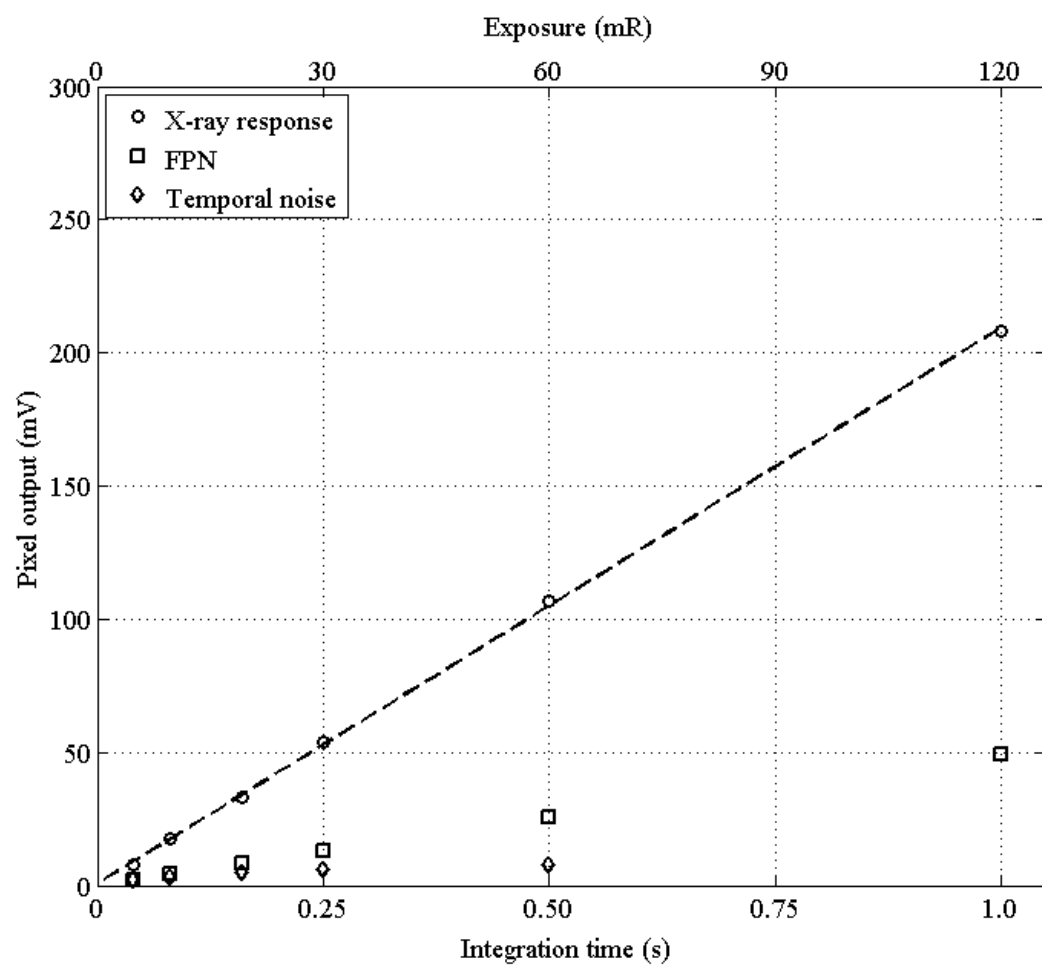


Figure 3.8: Quadrant 4 response versus integration time for all quadrants after flat field correction.

3.2.4 MTF Measurements

Figure 3.9 shows MTF measurements obtained using the slanted edge technique explained in [41]. The edge test device was made by machining the edge of a 3.5 mm thick lead block. The edge was imaged when aligned at a small angle relative to the array columns in order to determine MTF along the row direction. The MTF degrades by 50% at 23 mm^{-1} and 32 mm^{-1} spatial frequencies (corresponding to $22 \mu\text{m}$ and $16 \mu\text{m}$ object sizes) for the $11.2 \mu\text{m}$ and $5.6 \mu\text{m}$ pixel dimensions, respectively, and demonstrates the highest resolution direct conversion X-ray imager for diagnostic X-ray exposures reported to date. The measured MTF is compared to a model [35] which assumes ideal, normal X-ray incidence and does not take scattering and re-absorption effects into account. Sources of measurement error include edge imperfections and incident X-ray obliquity induced by source-imager misalignment.

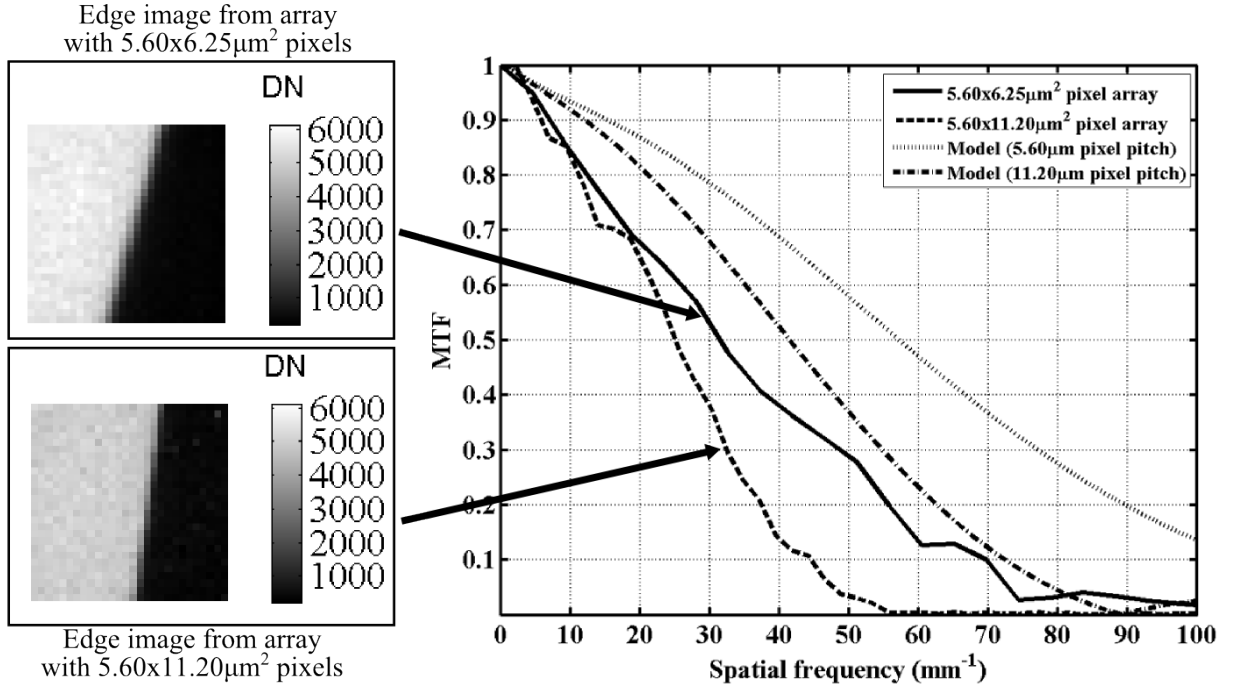


Figure 3.9: Measured (MTF) obtained from an X-ray edge image at 70kVp from Q1 and Q2 arrays with $5.60 \times 6.25 \mu\text{m}^2$ pixels. MTF of an array with $11.20 \times 6.25 \mu\text{m}^2$ pixels on the same chip has been included for comparison. Simulation results from a computational model of a-Se have also been included to show the maximum achievable MTFs for each array under ideal conditions.

3.2.5 Potential for Single Photon Counting

The smallest X-ray signal that a pixel can receive is one photon. If the system noise is less than the signal generated by one photon, further noise reduction is not necessary. If we assume the LOP occurs for $\text{SNR} = 1$, then the LOP for four arrays are equivalent with measured 139, 215, 118 and 99 electrons for 336 ms. So if the sensor produces this number of electrons per photon then the system is a single photon detecting imager. Equation 2.2 tells us the number of electrons depends on X-ray photon energy. With this equation (2.1) we can solve for the minimum detection energy for each array. The result is 13.1, 20.2, 11.1 and 9.3 keV photons for Q1, Q2, Q3 and Q4 respectively. This means if a photon with more energy than these gets absorbed by a-Se, the system can detect that photon.

3.3 Pixel Comparison

As one of the objectives of this project, we designed several pixel types to compare their performance. The 3T pixels in Q3 have the size advantage if MIM caps are not used in the design and this advantage is serious especially in optical imaging. In noise, Q3 plus have a better performance than pixels in Q1 and Q2. Pixels in Q4 have less noise but we have to note the reset voltage of this pixel is 1V higher than other pixels because of not using native transistor in source follower structure. This decreases the leakage at integration node and results in less noise. So we think because the noise increases with integration time based on measurements, shot noise is one of the most serious sources of noise. So at the end, 3T pixel is the main candidate for extending this project for bigger arrays.

3.4 X-ray Images

In this section we present several X-ray images taken with our a-Se/CMOS imager. The small pixel array sizes on the chip limit the size of the object we can image. therefore, we have used two objects that are reasonable for this scale. Figure 3.10 shows these images taken using Q1. The top one is the image of a loop of 50 μm diameter-copper wire (imaged at a 40-kVp tube voltage) and a stainless steel syringe tip (imaged at 70 kVp). In both cases, the tube current is 15 mA and the pixel integration time is 1.67 s. Although the clarity of these images at a resolution of 5.6 $\mu\text{m} \times 6.25 \mu\text{m}$ is apparent, there are mitigating factors including a lower than optimal a-Se sensor thickness and a non-optimized X-ray spectrum for imaging thin wires, reducing image quality.

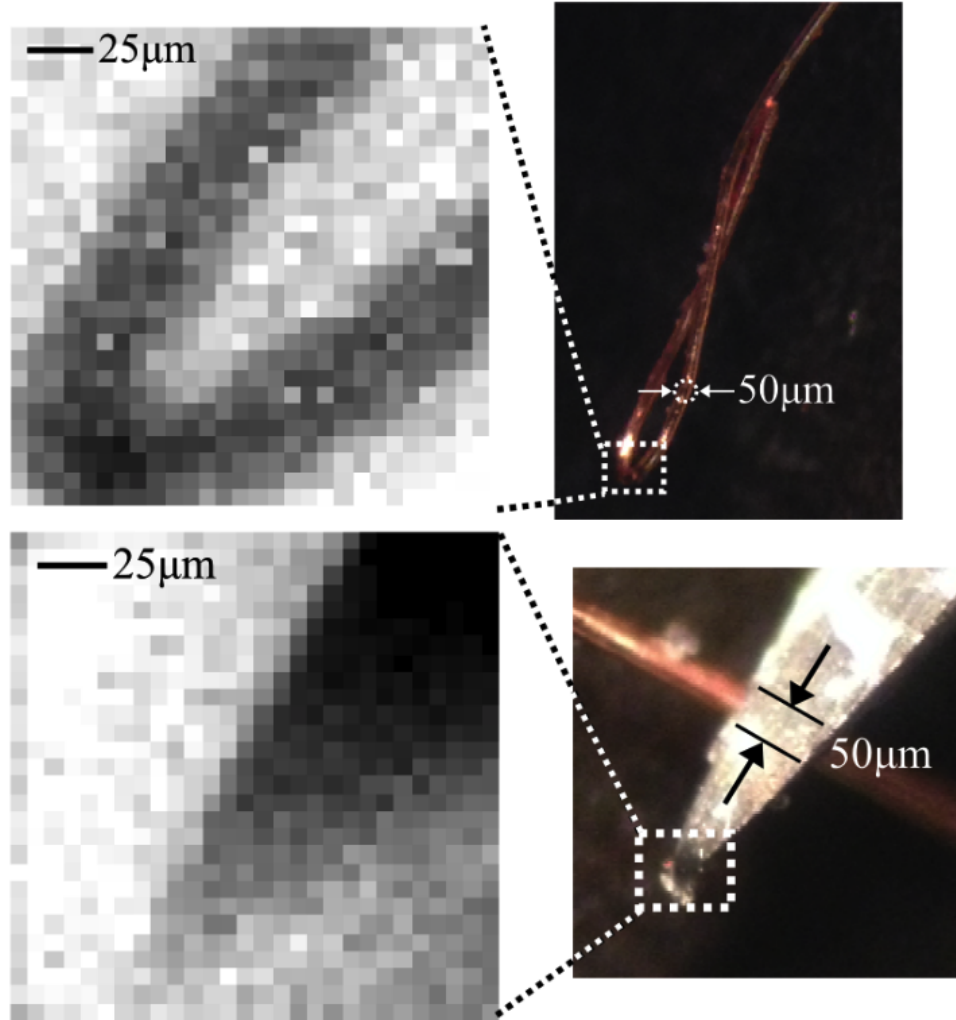


Figure 3.10: Flat field corrected X-ray images from 50 μm diameter copper and a needle tip taken using Q1.

Designing larger imagers is necessary for more practical imaging. Because the CMOS wafers are limited in area, special design techniques are used to achieve larger area imagers. One solution is tiling these small imagers which means putting lots of chips beside each other to form a bigger imager. This solution needs special layout design considerations for positioning the chips. The other solution which is acceptable for some applications is to

move the imager or object with an accurate system and take images in different positions and combine these images into a single larger image. This method was applied to our imager to show the feasibility of this solution. A $25\text{ }\mu\text{m}$ thick gold wire was wrapped around a piece of glass as dense as possible and the glass was mounted on a substrate with accurate position controlling. This device includes stepper motors with movement accuracy of $1\text{ }\mu\text{m}$ which is suitable for this experiment. Then 5 images were taken with 60 kVp X-ray photons with $140\text{ }\mu\text{m}$ displacing the object per image. The images were put together with slight position adjust and the result is shown in Figure 3.11. As we can see we covered area is larger than a single image.



Figure 3.11: Tiled image of $25\mu\text{m}$ wide gold wires using moving stage to get 5 images

Chapter 4

Conclusion

As expected, in some areas the imager does not have the performance that we designed for and in some areas it worked as it was designed. The most important feature is the resolution of this imager. This research shows the potential in combination of CMOS technology and direct X-ray conversion a-Se sensor that leads to a very high resolution X-ray imaging system. Note there are other systems like X-ray crystallography with atomic resolution, but it cannot be categorize in the same class as our imager .

The first reason is the area that those methods can cover is much smaller and cannot be scaled for other applications. But for this prototype the area can be scaled with increasing the CMOS size. Moreover, there are some techniques like tiling and line scanning which can be used to cover a large area. Also CMOS can operate really fast to take multiple images and combine them as one image. On the sensor side, all is done is a simple a-Se evaporation on surface of imaging circuit so extending the area does not introduce new serious challenges.

The second reason is simplicity of this design. X-ray crystallography machines use the diffraction angle of X-rays and based on that determine the structure. So taking an image needs accurate setup and it is sensitive to any vibration. The result is a high cost of production and imaging both, but the introduced technology does not need any special setup and the setup is like a conventional X-ray imager.

As a result in the class of biomedical X-ray imaging systems and other applications for larger area we can claim ultra high resolution direct-conversion imaging systems. This

claim can be supported by the MTF measurement shown in figure 3.9. This experimental result is not as good as ideal $5.6\text{ }\mu\text{m}\times 6.25\text{ }\mu\text{m}$ pixels and, as we can see in the plot the MTF drops faster which translates in larger effective pixel pitch. We believe the main reason of this difference is lack of accurate equipment used in this experiment. The algorithm used to measure MTF is based on some assumptions that was not guaranteed in our setup. The first one is an ideal edge object assumed in this method. The object we have used was mechanically polished lead block. The edge seems to be clean but under microscope lots of defects and bumps were observed on the edge. Note in $5.6\mu\text{m}$ scale any small defect can result in a considerable error. Also the photon projection direction should be perpendicular to surface of the object [35]. So the setup needs to be more accurate. This result shows the quantified metric of this imager resolution potential but for more accurate MTF measurement more equipments are necessary to reach high accuracy.

Imager speed is really important in some applications like X-ray tomosynthesis and video X-ray imagers like DALSA Xineos-FL CMOS flat X-ray detector. One of the serious limiting factors is the ADC clock signal. The ADC clock is 32 times faster than sampling rate. This is due to serial communication of this ADC. The clock generated by FPGA was probed by oscilloscope and it is not clean in high frequencies and distortion makes the edges of the signal undetectable and non-uniform. we suggest using an ADC with parallel output bits, for next PCB board generation which results in $\frac{1}{16}$ of the clock frequency of the ADC comparing with serial output.

The correlated double sampling does not improve the performance of the imager. We have applied the CDS experimentally on 4T arrays and the result has a higher noise in respect to non-CDS noise measurements for Q1 and Q4. For Q2 the result is almost same which has lower kT/C noise but other sources are added up in two samples and no improvement is achieved. The reason is explained and it is shown that this design suffers from kTC noise.

4.1 Future Work

There are several main paths to continue this research and investigation on a-Se. One is to add a blocking layer to the a-Se sensor. It is shown in our group adding a blocking layer to a-Se can boost the performance by decreasing dark current and reaching high gain under high voltage [2]. The other investigation can be done by increasing the a-Se biasing voltage and operate it in avalanche mode. In this mode, the sensor response is not the same and other investigations are necessary to study the imager. Also each application

has different energy of X-ray photons. The thickness of a-Se layer can be optimized if a specific application is the target for this system.

On the CMOS side, the pixel pitch can be reduced more. There are new challenges like using another kind of pixel capacitance instead of MIM capacitors or working with transistor parasitic capacitance which might result in much larger FPN. To shrink down more, other CMOS technologies can be used with smaller gate length like 65 nm. There are serious concerns about leakages in those technologies that needs to be addressed.

In terms of system level CMOS design, for next generation of this chip one buffer per column is necessary if higher number of pixels is the target. Also the ADC can be integrated on chip. With on-chip ADC the data output from the chip is digitized and therefore is less sensitive to interference from PCB components. However, designing an ADC with high speed and more than 12 bit resolution is challenging.

In the system level, there are other standard specifications for an imager which quantify the performance. For example detective quantum efficiency (DQE) and noise power spectrum (NPS) can be measured experimentally [28]. Also, because the ratio between pixel pitch to sensor thickness is only $\frac{6.25\mu m}{60\mu m} = 0.1$ we expect to see “small pixel effect”. This phenomenon makes the system independent of hole drift and results in single carrier detection [48] however, more experimental data is necessary to confirm this effect in our imager.

Appendix A

PCB Schematic

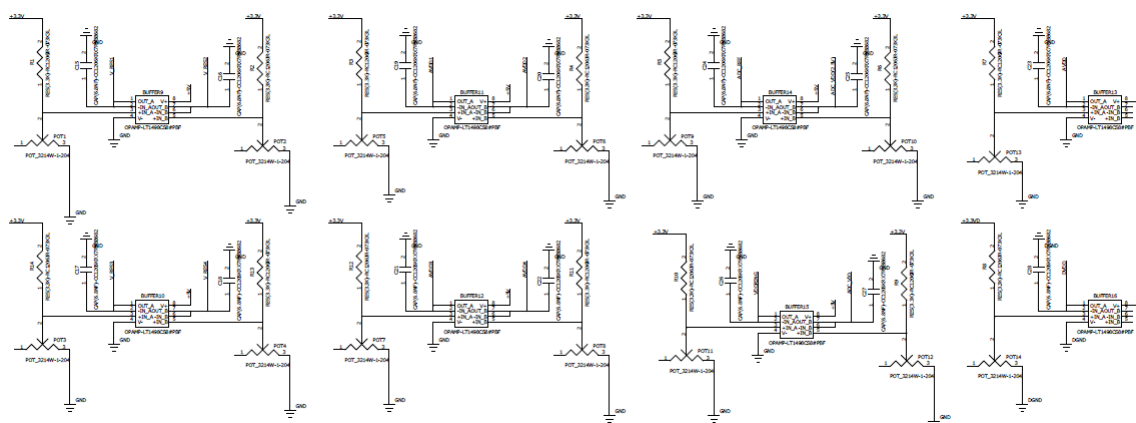


Figure A.1: Biasing circuitry in PCB top level schematic

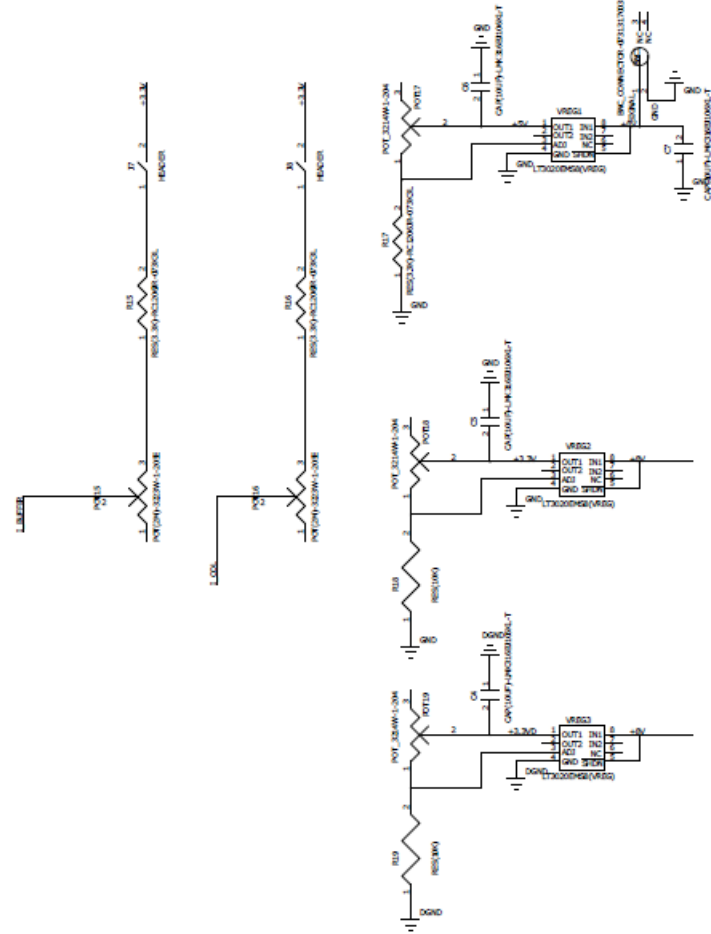


Figure A.2: Power circuitry in PCB top level schematic

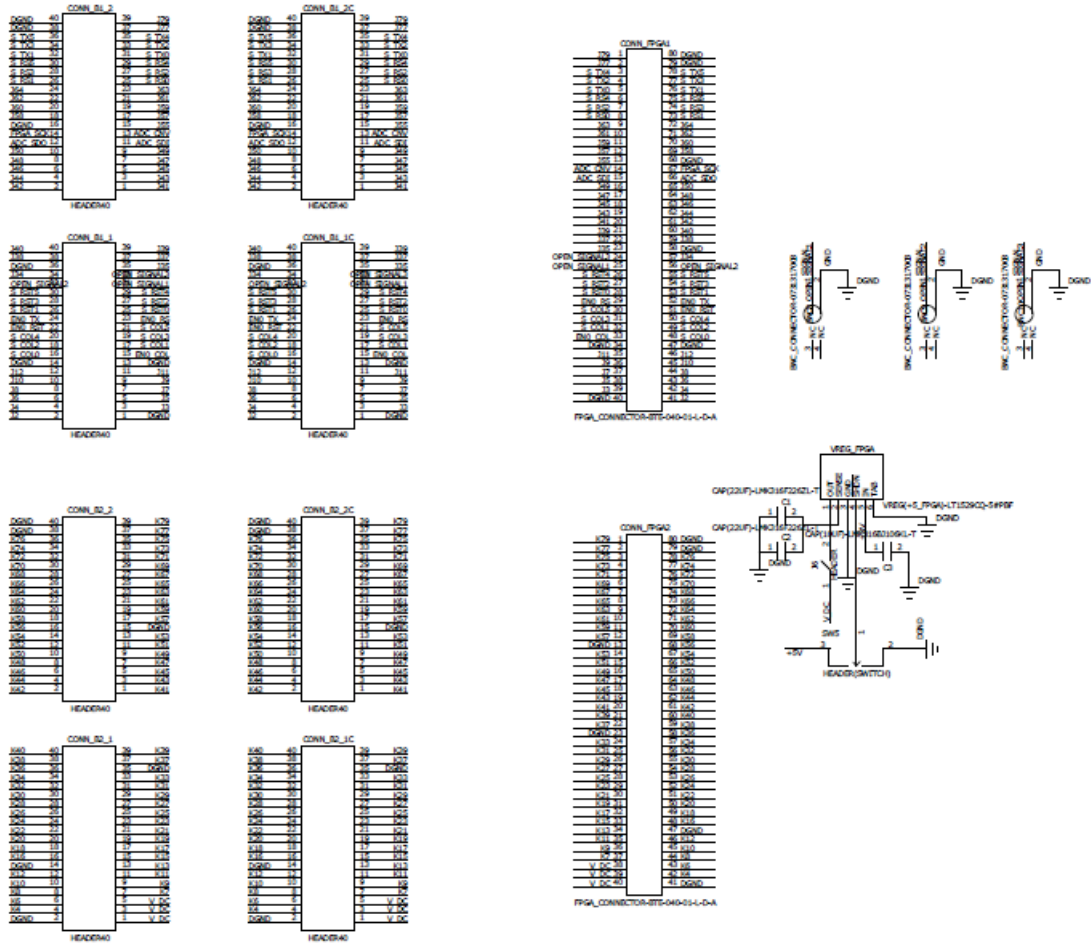


Figure A.4: Digital connectors in PCB top level schematic

Appendix B

CMOS Chip Pinout

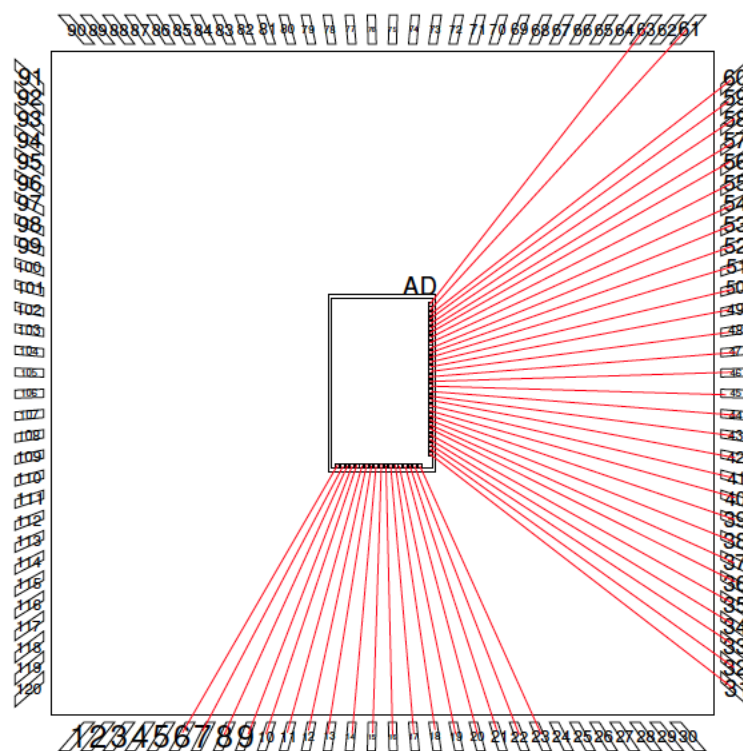


Figure B.1: CMOS chip bonding diagram

Pin number	Name	Direction	Description
6	NC	NA	
7	Bypass_Out	Out	System output when on chip buffer is bypassed.
8	I_Col	In	Pixel Source Follower Biasing current. 22.5 uA DC current should be provided.
9	I_Buffer	In	On-chip buffer Biasing current. 100 uA DC current should be provided.
10	Bypass	In	Bypass signal to bypass the on-chip buffer. Connect to 3.3V to enable bypass operation.
11	Out	Out	Output of the system in normal operation (Not bypass)
12	V_Res4	In	Quadrant 4 pixel reset voltage (1.4 V)
13	V_Res3	In	Quadrant 3 pixel reset voltage (0.4 V)
14	V_Res2	In	Quadrant 2 pixel reset voltage (0.4 V)
15	V_Res1	In	Quadrant 1 pixel reset voltage (0.4 V)
16	AVDD4	In	Quadrant 4 pixel VDD Voltage (3.3 V)
17	AVDD3	In	Quadrant 3 pixel VDD Voltage (3.3 V)
18	AVDD2	In	Quadrant 2 pixel VDD Voltage (3.3 V)
19	AVDD1	In	Quadrant 1 pixel VDD Voltage (3.3 V)
20	GND	In	Ground
21	AVDD	In	Analog VDD Voltage (3.3 V)
22	GND	In	Ground
23	VDDRing	In	Chip pads protection voltage (3.3 V)
31	S_TX5	In	4T pixels tranmission adress 5th bit (MSB)
32	S_TX4	In	4T pixels tranmission adress 4th bit
33	S_TX3	In	4T pixels tranmission adress 3rd bit
34	S_TX2	In	4T pixels tranmission adress 2nd bit
35	S_TX1	In	4T pixels tranmission adress 1st bit
36	S_TX0	In	4T pixels tranmission adress LSB bit
37	S_RS5	In	Pixels row select adress 5th bit (MSB)

Pin number	Name	Direction	Description
38	S_RS4	In	Pixels row select address 4th bit
39	S_RS3	In	Pixels row select address 3rd bit
40	S_RS2	In	Pixels row select address 2nd bit
41	S_RS1	In	Pixels row select address 1st bit
42	S_RS0	In	Pixels row select address LSB bit
43	S_RST5	In	Pixels row reset address 5th bit (MSB)
44	S_RST4	In	Pixels row reset address 4th bit
45	S_RST3	In	Pixels row reset address 3rd bit
46	S_RST2	In	Pixels row reset address 2nd bit
47	S_RST1	In	Pixels row reset address 1st bit
48	S_RST0	In	Pixels row reset address LSB bit
49	ENO_TX	In	Enable(inversed)of 4T pixels tranmission addressing
50	ENO_RS	In	Enable (inversed)of row select addressing
51	ENO_RST	In	Enable (inversed)of row reset addressing
52	DVDD	In	Digital VDD (3.3 V)
53	GND	In	Ground
54	DVDD	In	Digital VDD (3.3 V)
55	GND	In	Ground
56	S_COL5	In	Pixels column select address 5th bit (MSB)
57	S_COL4	In	Pixels column select address 4th bit
58	S_COL3	In	Pixels column select address 4th bit
59	S_COL2	In	Pixels column select address 4th bit
60	S_COL1	In	Pixels column select address 4th bit
61	S_COL0	In	Pixels column select address 4th bit
63	ENO_COL	In	Enable (inversed)of column select addressing

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